

The diagram illustrates the system architecture for the Intel Atom Z670. At the center is the **PCH Ibex Peak-M** (Page 20-28), which connects to various components:

- CPU Arrandale (DC)** (Page 3-7) is connected via **PCIe x16** and **DDR3 1333MHz** to **DDR3 SO-DIMM** (Page 16-18).
- Storage and Expansion:**
 - MiniCard WLAN Shirley Peak/ Echo Peak** (Page 53) and **MiniCard HSPA (3G)** (Page 64) are connected via **PCIe x1**.
 - GigaLAN AR8131** (Page 33-34) is connected via **USB** to an **RJ45** port (Page 34).
 - ExpressCard** (Page 43) is connected via **PCIe x1**.
 - USB Ports (1, 2, 3)** (Pages 52, 52, 52) are connected via **USB**.
 - Bluetooth** (Page 61) and **CMOS Camera** (Page 45) are connected via **USB**.
 - Storage:** **ODD** (Page 51), **HDD(1)** (Page 51), and **eSATA** (Page 66) are connected via **SATA**.
- Peripherals and Sensors:**
 - Debug Conn.** (Page 44) and **EC ITE IT8512E** (Page 30) are connected via **LPC**.
 - EC ITE IT8512E** is also connected to **SPI ROM** (Page 28) and **SPI ROM** (Page 30) via **SPI**.
 - Thermal Sensor PWM Fan** (Page 50) is connected via **SMbus**.
 - CardReader Alcor AU4633** (Page 40-41) is connected via **PCIe x1**.
 - Azalia Codec Realtek ALC269** (Page 36) is connected via **Azalia** to **Speaker** (Page 37) and **Audio Jack** (Page 65).
 - Clock Generator ICS ICS9LRS3197** (Page 29) is connected via **SMbus**.
- Other Components:**
 - HDMI** (Page 48) and **SDVO** (Page 48) are connected via **HDMI**.
 - CRT** (Page 46) and **LCD Panel** (Page 45) are connected via **LVDIS** and **CRT**.
 - Touchpad Keyboard** (Page 31) is connected via **LPC**.
 - Discharge Circuit** (Page 57), **Reset Circuit** (Page 32), **DC & BATT. Conn.** (Page 60), and **Skew Holes** (Page 65) are shown at the bottom.

PCH_IBEX GPIO

PCH_IBEX GPIO	Use As	Signal Name	Internal & External Pull-up/down	Power
GPIO 00	-	GPIO0	-	+3VS
GPIO 01	-	DOCKING_DET#	EXT PU	+3VS
GPIO [2:5]	Native	PCI_INT[E:H]#	EXT PU	+5VS
GPIO 06	-	DGPU_PWR_EN	EXT PU	+3VS
GPIO 07	-	XIDE_BAY_IN#	EXT PU	+3VS
GPIO 08	GPI	EXT_SMI#	EXT PU & INT PU	+3VSUS
GPIO 09	Native	USB_OC5#	EXT PU	+3VSUS
GPIO 10	Native	USB_OC6#	EXT PU	+3VSUS
GPIO 11	GPI	EXT_SCI#	EXT PU	+3VSUS
GPIO 12	-	PM_LANPHY_EN	EXT PU	+3VSUS
GPIO 13	-	DGPU_PWR_EN_R	-	+3VSUS
GPIO 14	Native	USB_OC7#	EXT PU	+3VSUS
GPIO 15	GPO	BT_LED	INT PD	+3VSUS
GPIO 16	-	DGPU_HOLD_RST#	-	+3VS
GPIO 17	-	DGPU_PWR_OK	EXT PD & INT TBD	+3VS
GPIO 18	-	CLK_REQ1#	EXT PU(DNI)/PD	+3VS
GPIO 19	Native	SATA1GP	-	+3VS
GPIO 20	Native	CLKREQ2_WLAN#	EXT PU(DNI)/PD	+3VS
GPIO 21	Native	SATA0GP	-	+3VS
GPIO 22	GPO	WLAN_LED	EXT PD	+3VS
GPIO 23	-	LPC_DRQ#1	-	+3VS
GPIO 24	-	OC_LAN_RST#	EXT PU	+3VSUS
GPIO 25	Native	CLKREQ3_NEWCARD#	EXT PU(DNI)/PD	+3VSUS
GPIO 26	-	CLK_REQ4#	EXT PU(Not used)	+3VSUS
GPIO 27	-	VRM_EN	INT WEAK PU	+3VSUS
GPIO 28	GPO	WLAN_ON	EXT PD	+3VSUS
GPIO 29	Native	ME_PM_SLP_LAN#	EXT PU(DNI)/PD(DNI)	+3VSUS
GPIO 30	Native	ME_SUSPWRDNACK	EXT PU	+3VSUS
GPIO 31	Native	ME_AC_PRESENT	EXT PU	+3VSUS
GPIO 32	Native	PM_CLKRUN#	EXT PU	+3VS
GPIO 33	Native	HDA_DOCK_EN#	-	+3VS
GPIO 34	Native	STP_PCI#	EXT PU	+3VS
GPIO 35	GPO	CAP_RST#_ICH	EXT PU/PD(DNI)	+3VS
GPIO 36	-	DGPU_PWR_EN#	EXT PU	+3VS
GPIO 37	-	DGPU_PRSTNT#	EXT PU	+3VS
GPIO 38	GPI	PCB_ID0	EXT PD	+3VS
GPIO 39	GPI	PCB_ID1	EXT PD	+3VS
GPIO 40	Native	USB_OC1#	EXT PU (Not used)	+3VSUS
GPIO 41	Native	USB_OC2#	EXT PU (Not used)	+3VSUS
GPIO 42	Native	USB_OC3#	EXT PU (Not used)	+3VSUS
GPIO 43	Native	USB_OC4#	EXT PU (Not used)	+3VSUS
GPIO 44	Native	CLK_REQ5_LAN#	EXT PU (Not used)	+3VSUS
GPIO 45	-	CLK_REQ6#	EXT PU (Not used)	+3VSUS
GPIO 46	-	CLK_REQ7#	EXT PU (Not used)	+3VSUS
GPIO 47	-	CLKREQ_PEG#	EXT PD	+3VSUS
GPIO 48	-	EMAIL_LED	-	+3VS
GPIO 49	GPO	PCH_TEMP_ALERT#	-	+3VS
GPIO 50	-	PCI_REQ1#	EXT PU (Not used)	+5VS
GPIO 51	-	PCI_GNT1#	INT PU	+3VS
GPIO 52	-	PCI_REQ2#	EXT PU	+5VS
GPIO 53	-	PCI_GNT2#	INT PU	+3VS
GPIO 54	-	PCI_REQ3#	INT PU	+5VS
GPIO 55	Native	PCI_GNT3#	INT PU	+3VS
GPIO 56	Native	CLKREQ_GLAN#_R	EXT PU(DNI)/PD	+3VSUS
GPIO 57	GPO	BT_ON	EXT PU(DIODE)	+3VSUS
GPIO 58	Native	SML1_CLK	EXT PU	+3VSUS
GPIO 59	Native	USB_OC0#	EXT PU (Not used)	+3VSUS
GPIO 60	-	RTLAN_DSM_EN	EXT PU	+3VSUS
GPIO 61	-	PM_SUS_STAT#	-	+3VSUS
GPIO 62	-	SUS_CLK	-	+3VSUS
GPIO 63	-	SLP_S5#	-	+3VSUS
GPIO 64	-	CLK_OUT0	INT TBD	+3VS
GPIO 65	-	CLK_OUT1	INT TBD	+3VS
GPIO 66	-	CLK_OUT2	INT TBD	+3VS
GPIO 67	Native	CLK_USB48_CR	INT TBD	+3VS
GPIO 72	-	PM_BATLOW#	EXT PU (Not used)	+3VSUS
GPIO 73	-	CLK_REQ0#	EXT PU (Not used)	+3VSUS
GPIO 74	-	SML1ALERT#	EXT PU (Not used)	+3VSUS
GPIO 75	Native	SML1_DAT	EXT PU	+3VSUS

EC IT8512

EC GPIO	Use As	Signal Name
GPIO0	O	PWR_LED#
GPA1	O	CHG_LED#
GPA2	-	-
GPA3	-	-
GPA4	O	LCD_BL_PWM
GPA5	O	FAN_PWM
GPA6	-	-
GPA7	-	-
GPB0	-	-
GPB1	-	-
GPB2	-	-
GPB3	IO	SMB0_CLK
GPB4	IO	SMB0_DAT
GPB5	O	A20GATE
GPB6	O	RCIN#
GPB7	O	PM_RSMRST#
GPC0	-	-
GPC1	IO	SMB1_CLK
GPC2	IO	SMB1_DAT
GPC3	O	PM_PWRBTN#
GPC4	I	AC_IN_OC#
GPC5	O	OP_SD#
GPC6	I	BAT1_IN_OC#
GPC7	I	RFON_SW#
GPD0	I	PWRLIMIT#
GPD1	I	PM_SUSC#
GPD2	I	BUF_PLT_RST#
GPD3	O	EXT_SCI#
GPD4	O	EXT_SMI#
GPD5	O	LCD_BACKOFF#
GPD6	I	FAN0_TACH
GPD7	-	-
GPE0	O	VSUS_ON
GPE1	O	SUSC_EC#
GPE2	O	SUSB_EC#
GPE3	O	CPU_VRON
GPE4	I	PWR_SW#
GPE5	-	-
GPE6	I	LID_SW#
GPE7	I	CAP_ACK#
GPFO	-	-
GPF1	-	-
GPF2	-	-
GPF3	I	DISTP#
GPF4	I	TP_CLK
GPF5	IO	TP_DAT
GPF6	O	THRO_CPU
GPF7	O	ME_AC_PRESENT
PGFO	O	KB_ID0
GPG1	I	PM_SUSB#
GPG2	-	-
GPG6	-	-
GPH0	IO	PM_CLKRUN#
GPH1	I	3G_ON
GPH2	O	GEX_VR_ON
GPH3	-	-
GPH4	-	-
GPH5	-	-
GPH6	O	CAP_LED#
GPI0	I	PCH_TEMP_ALERT#
GPI1	I	SUS_PWRGD
GPI2	I	ALL_SYSTEM_PWRGD
GPI3	I	VRM_PWRGD
GPI4	I	ME_PM_SLP_LAN#
GPI5	-	-
GPI6	I	ME_PM_SLP_M#
GPI7	I	ME_SUSPWRDNACK
GPJ0	O	CAP_RST#_EC
GPJ1	O	PM_PWROK
GPJ2	O	KB_ID1
GPJ3	-	-
GPJ4	O	TP_LED
GPJ5	I	GFX_VR

EC IT8301

EC GPIO	Use As	Signal Name
GPIO0	-	-
GPIO1	-	-
GPIO2	-	-
GPIO3	-	-
GPIO4	-	-
GPIO5	-	-
GPIO6	-	-
GPIO7	-	-
GPIO8	-	-
GPIO9	-	-
GPIO10	-	-
GPIO11	-	-
GPIO12	-	-
GPIO13	-	-
GPIO14	-	-
GPIO15	-	-
GPIO16	-	-
GPIO17	-	-
GPIO18	-	-
GPIO19	-	-
GPIO20	-	-
GPIO21	-	-
GPIO22	-	-
GPIO23	-	-
GPIO24	-	-
GPIO25	-	-
GPIO26	-	-
GPIO27	-	-
GPIO28	-	-
GPIO29	-	-
GPIO30	-	-
GPIO31	-	-
GPIO32	-	-
GPIO33	-	-
GPIO34	-	-
GPIO35	-	-
GPIO36	-	-
GPIO37	-	-

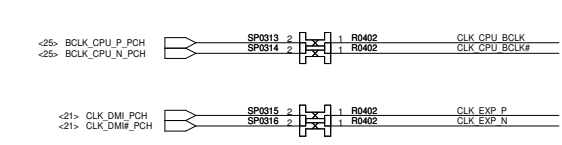
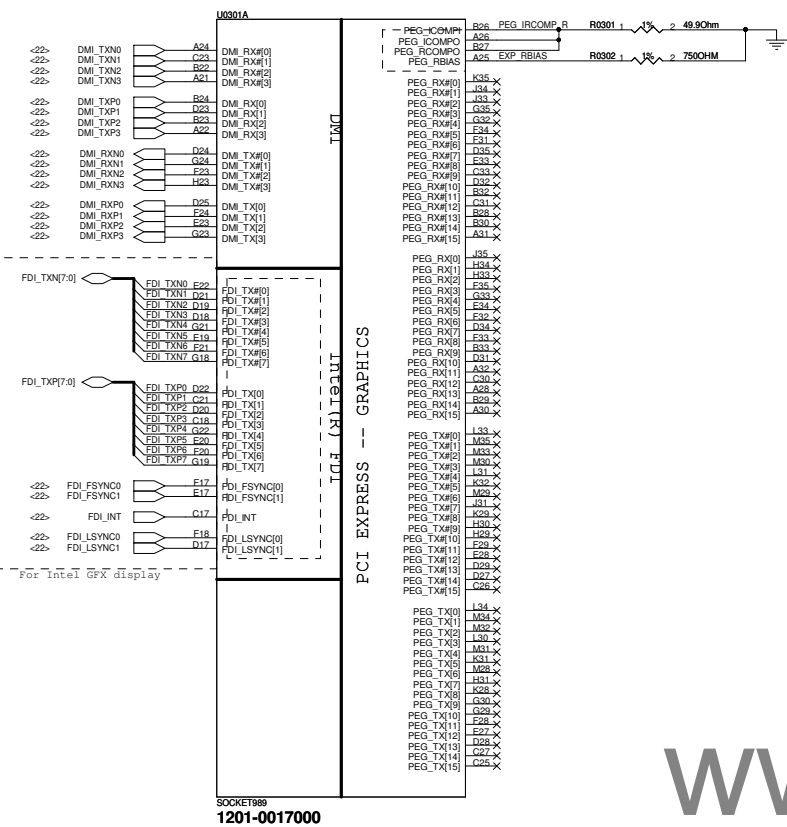
SM_BUS ADDRESS :

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x (D2h)
SO-DIMM 0	1010000x (A0h)
SO-DIMM 1	1010001x (A4h)
CPU Thermal IC(G780)	1001100x (98h)
VGA Thermal IC(G781-1)	1001101x (9Ah)
VGA Thermal Sensor(NB9E-GE1)	1001111x (9Eh)
VID Controller ASM8272	0011011x (36h)

PCIE 1	N/A
PCIE 2	Minicard WLAN
PCIE 3	Newcard
PCIE 4	N/A
PCIE 5	N/A
PCIE 6	GLAN
PCIE 7	N/A
PCIE 8	N/A

SATA0	SATA HDD
SATA1	SATA ODD
SATA2	N/A
SATA3	N/A
SATA4	N/A
SATA5	eSATA

USB 0	USB Port (1)
USB 1	USB Port (2)
USB 2	USB Port (3)
USB 3	N/A
USB 4	N/A
USB 5	Newcard
USB 6	Card Reader
USB 7	3G
USB 8	N/A
USB 9	WLAN
USB 10	N/A
USB 11	N/A
USB 12	Bluetooth
USB 13	CMOS Camera

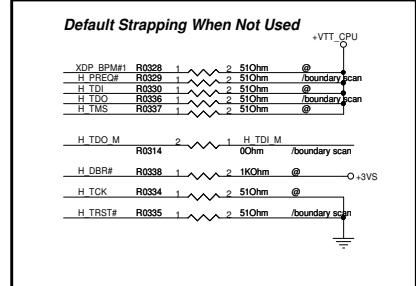


FDI disable: (For discrete graphic)

- 1. NC:**
FDI_TX#(0:7), FDI_TX#(0:7), FDI_RX#(0:7), FDI_RX#(0:7)
VCC_AXGSENSE, VSS_AXGSENSE
- 2. Pull-down to GND via 1KΩ ± 5% resistor:**
FDI_FSYNC(0:1), FDI_LSYNC(0:1), FDI_INT, GFX_IMON
~15mW power saving. (DG R0.8 P.70)
- 3. Connected to GND:**
VCCAXG, DPLL_REF_CLK, DPLL_REF_CLK#
- 4. Can be connected to GND directly:**
DPLL_REF_CLK, DPLL_REF_CLK#
- 5. Connect to +V1.05S rail:**
VCCFDIPLL

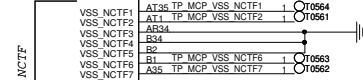
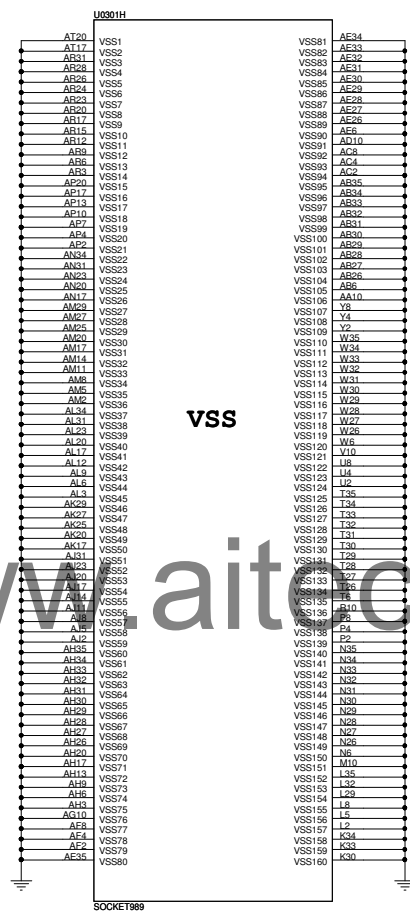
DRAMPWROK: (WW35 MoW)
Choose either one solution: --> Choose solution 2

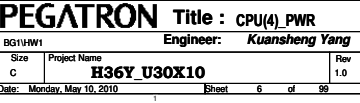
- This pin should have an external pull-up of 1K Ohms to 10K Ohms to a rail of 1.05/1.1V which is ON in S0-S3
- Connect this pin through a voltage divider circuit; recommend 4.75K Ohms pull-up to DDR3 Power Rail (VDDQ) of +V1.5U and a 12K Ohms pull-down to ground to convert to processor's VTT level.



Adding layout test point for boundary scan
Jervis 2009/11/09

CLK CPU BCLK	T0312
H_VTTPWRGD_R	T0313
VCCPWROOD_0_R	T0314
VCCPWROOD_1_R	T0315
PLT_RST#_R	T0316
H_TRST#	T0317
H_TCK	T0318
H_TMS	T0319
H_TDO	T0320
H_TDO_M	T0321
H_TDO_M	T0322
H_TDO_M	T0323





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PEGATRON		Title : CPU(5)_XDP	
BG1VHW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y U30X10		1.0
Date: Monday, May 10, 2010		Sheet	7 of 99

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PEGATRON		Title : NB(1) ****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	8 of 99

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PEGATRON		Title : NB(2)_****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	9 of 99

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PEGATRON		Title : NB(3) ****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	10 of 99

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PEGATRON		Title : NB(4) ****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	11 of 99

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PEGATRON		Title : NB(5) ****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	12 of 99

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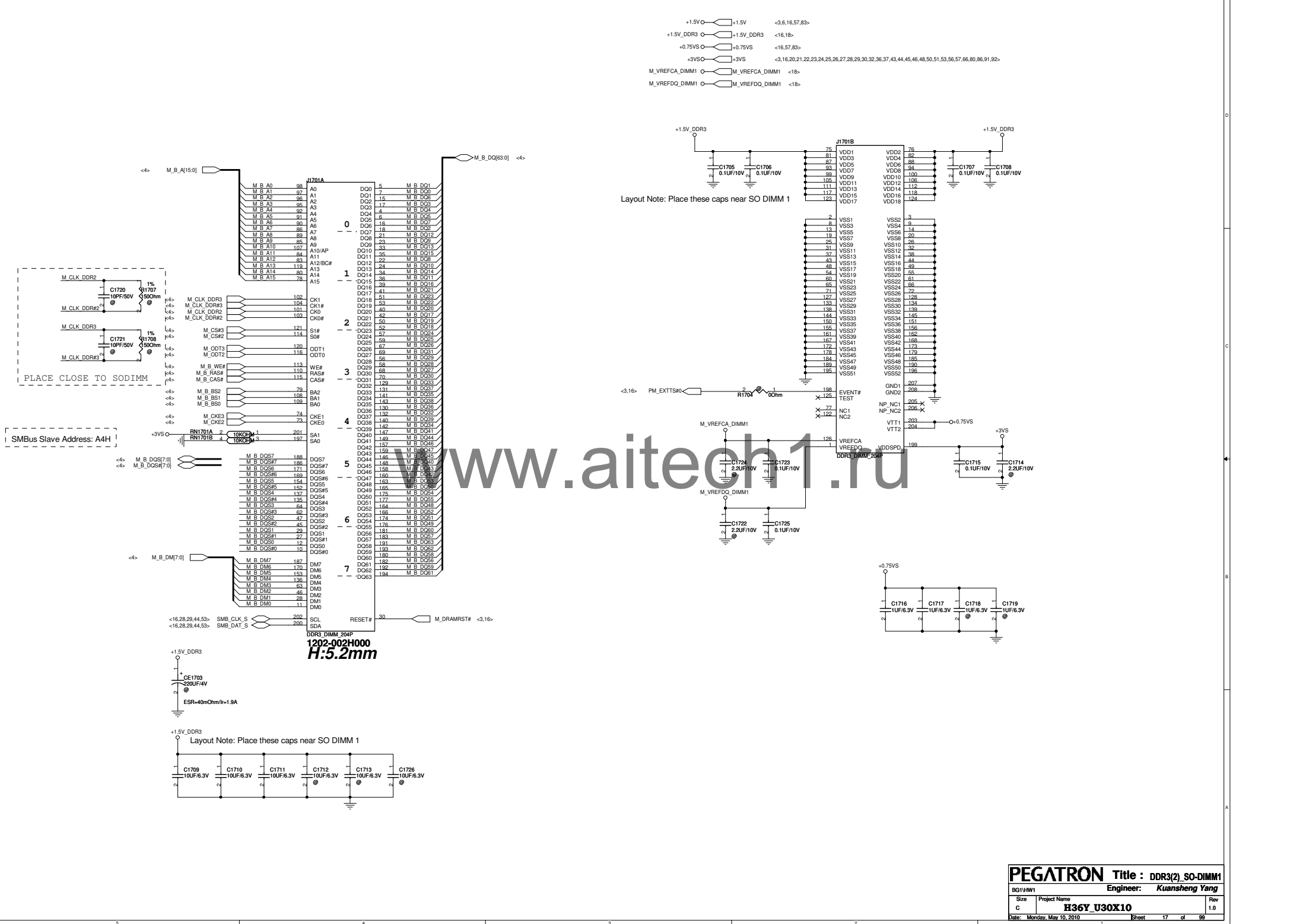
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BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
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Date: Monday, May 10, 2010		Sheet	13 of 99

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PEGATRON		Title : NB(7)_****	
BG1\HW1		Engineer: Kuansheng Yang	
Size A	H36Y_U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	14 of 99

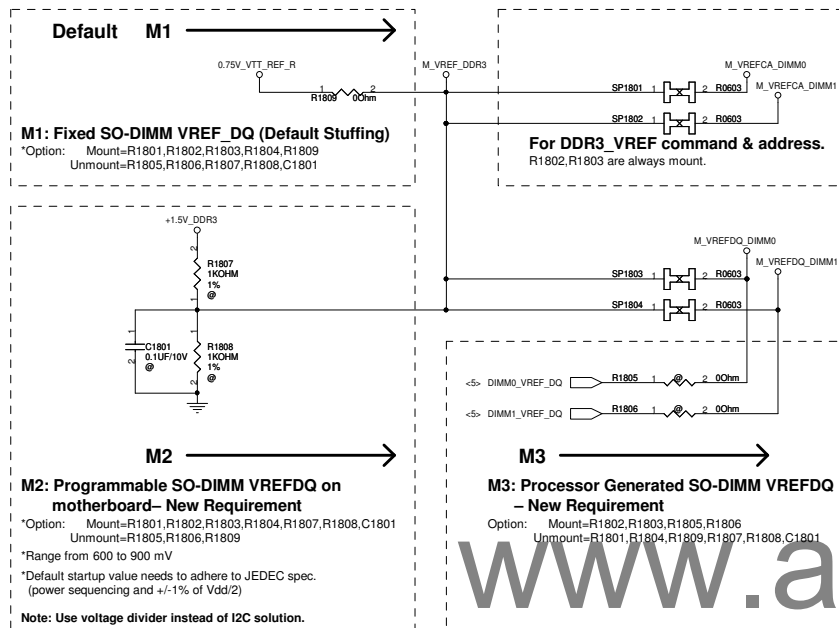
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PEGATRON		Title : NB(8) ****	
BG1\HW1		Engineer: Kuansheng Yang	
Size A	H36Y_U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	15 of 99



DDR3 Vref

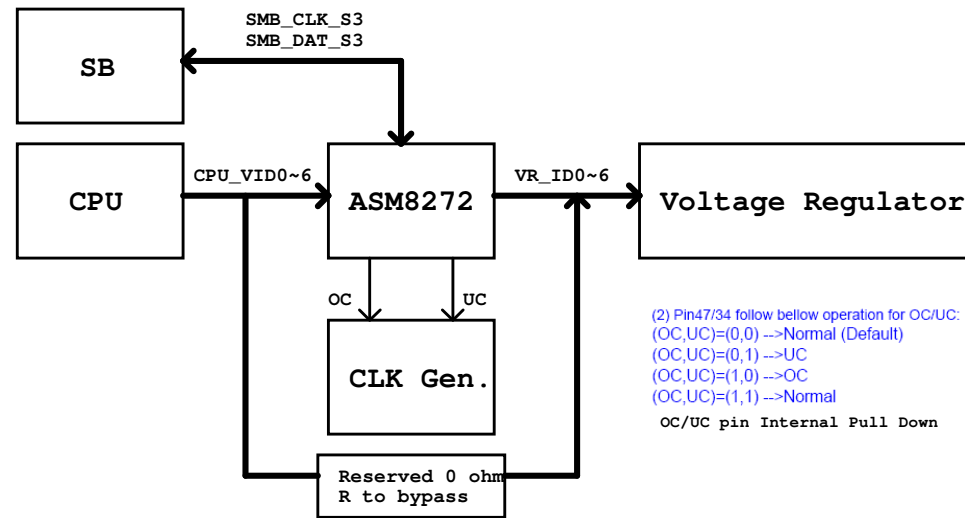
Intel Document Number: 400755
Calpella Clarksfield DDR3 SO-DIMM VREFDQ
Platform Design Guide Change Details



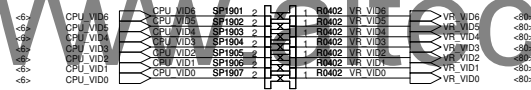
+1.5V_DDR3 <16,17>
M_VREFCA_DIMM0 <16>
M_VREFDQ_DIMM0 <16>
M_VREFCA_DIMM1 <17>
M_VREFDQ_DIMM1 <17>
+3V <24,33,40,43,45,53,54,56,57,61,91>
0.75V_VTT_REF_R <83>

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Block Diagram

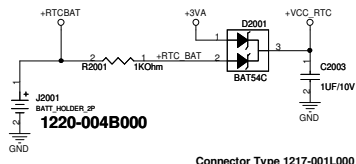


+VTT_CPU +VTT_CPU <3,6,25,26,32,57,82>
+3VSO +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>



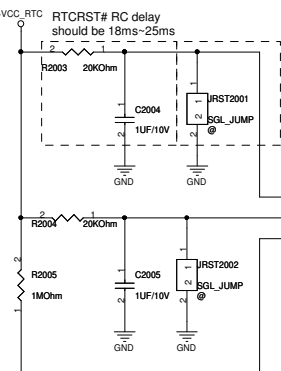
R1.4--2

RTC battery



Request by CSC
for CMOS clear
function

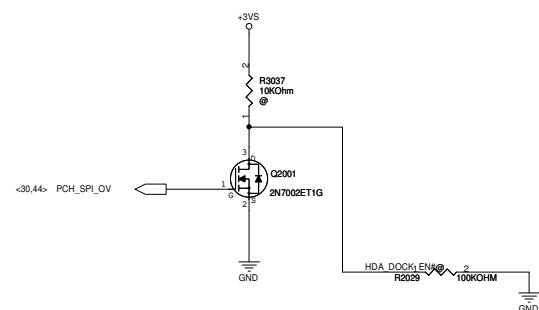
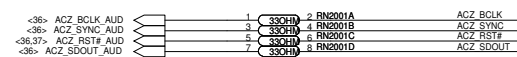
CMOS Settings	JRST2001
Clear CMOS	Shunt
Keep CMOS	Open (Default)



Adding layout test point
for boundary scan
Jervis 2009/11/09

TPM Settings	JRST2002
Clear ME RTC Registers	Shunt
Keep ME RTC Registers	Open (Default)

HDA_SYNC: Select VCCVPM 1.5V or 1.8V

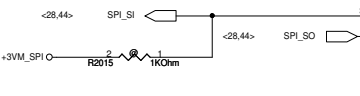
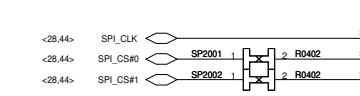
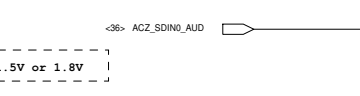
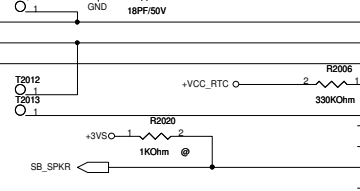
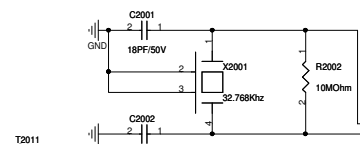
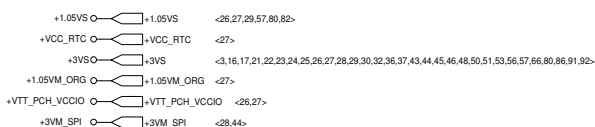


Strap information:

HDA_SPKR: No reboot strap
Low: Disable.
High: Enable

HDA_DOCK_EN#:
1. Flash descriptor security:
Sampled low: override
Sampled high: in effect.
2. GPIO33 low on the rising edge of PWROK,
Will also disable Intel ME.

SPI_MOSI: iTPM strap.
Mount R2015: Enable
Unmount R2015: Disable (default)



U2001A

RTCX1

RTCX2

RTCX3

RTCX4

RTCX5

RTCX6

RTCX7

RTCX8

RTCX9

RTCX10

RTCX11

RTCX12

RTCX13

RTCX14

RTCX15

RTCX16

RTCX17

RTCX18

RTCX19

RTCX20

RTCX21

RTCX22

RTCX23

RTCX24

RTCX25

RTCX26

RTCX27

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RTCX175

RTCX176

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RTCX178

RTCX179

RTCX180

RTCX181

RTCX182

RTCX183

RTCX184

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RTCX197

RTCX198

RTCX199

RTCX200

RTCX201

RTCX202

RTCX203

RTCX204

RTCX205

RTCX206

RTCX207

RTCX208

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RTCX211

RTCX212

RTCX213

RTCX214

RTCX215

RTCX216

RTCX217

RTCX218

RTCX219

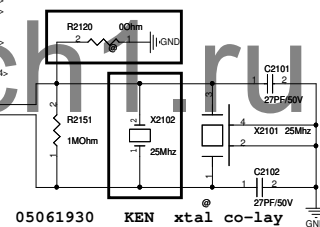
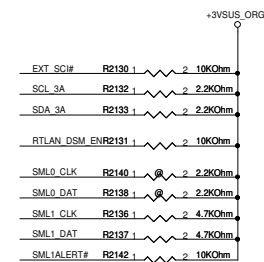
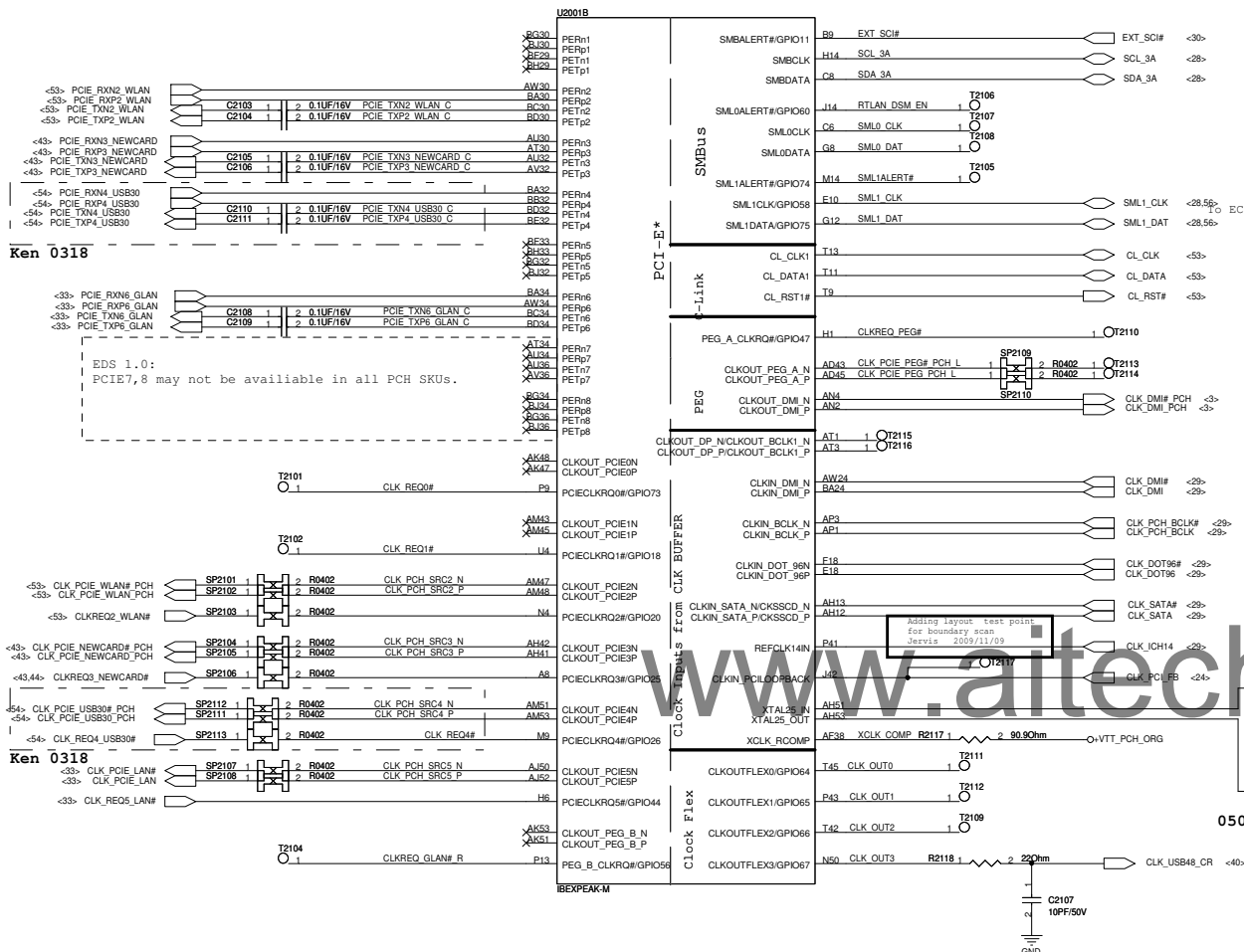
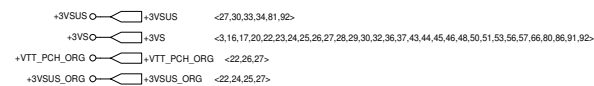
RTCX220

RTCX221

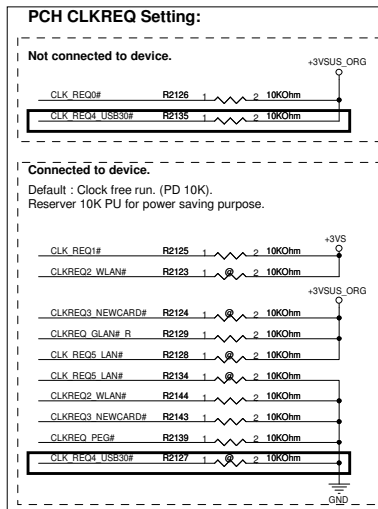
RTCX222

RTCX223

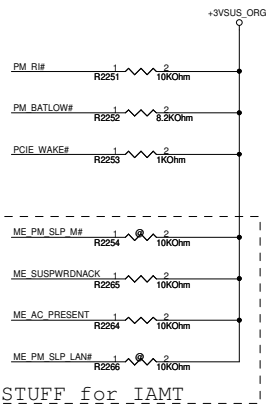
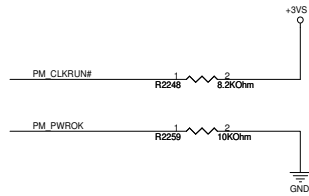
RTCX22



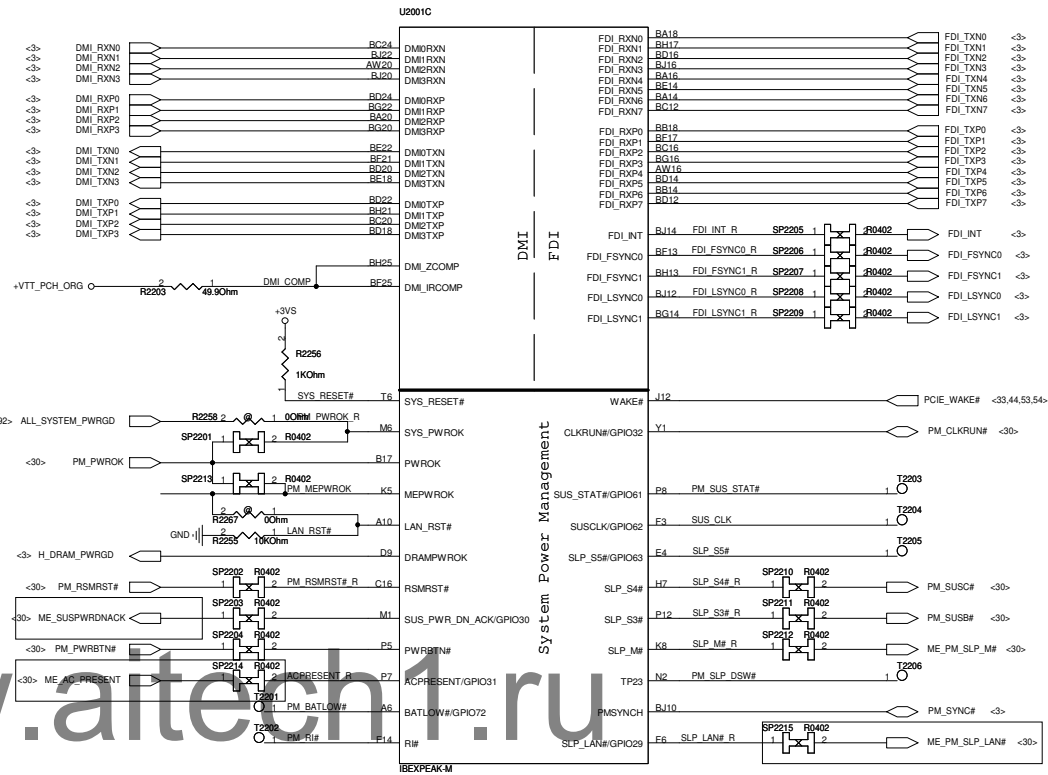
05061930 KEN xtal co-lay GND

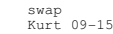
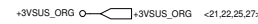


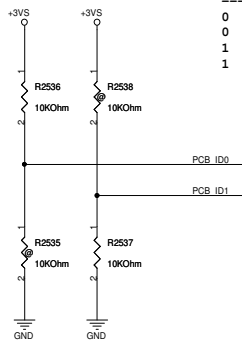
```
pre-ES1 not support
Reversal Feature
```



Adding layout test point
for boundary scan
Jervis 2009/11/09

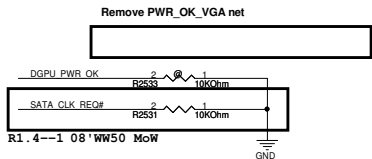
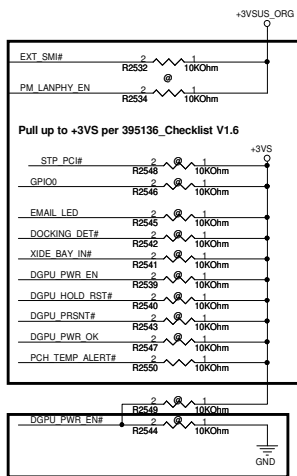
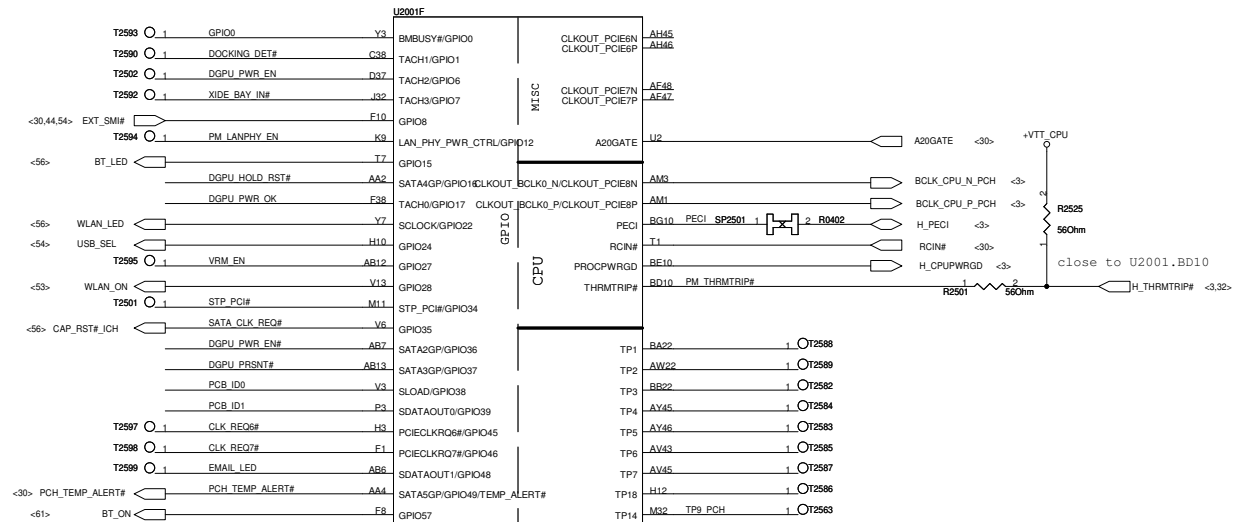






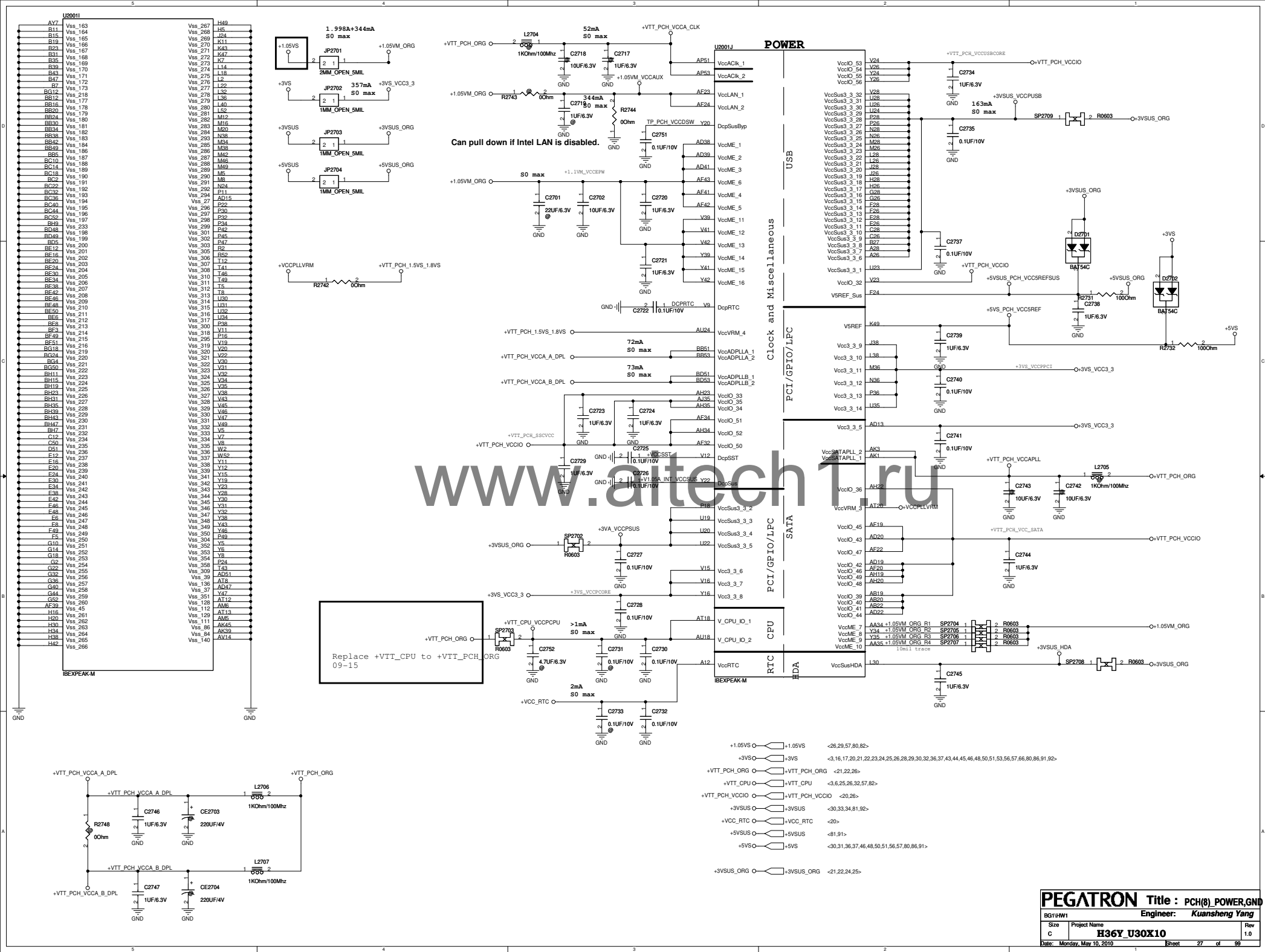
ID0	ID1	SKU
0	0	CFD_Non-IAMT
0	1	CFD_IAMT
1	0	AUB_Non-IAMT
1	1	AUB_IAMT

GPIO 27: Enable VCCVRM, Low=disable.
Default internal pull up.

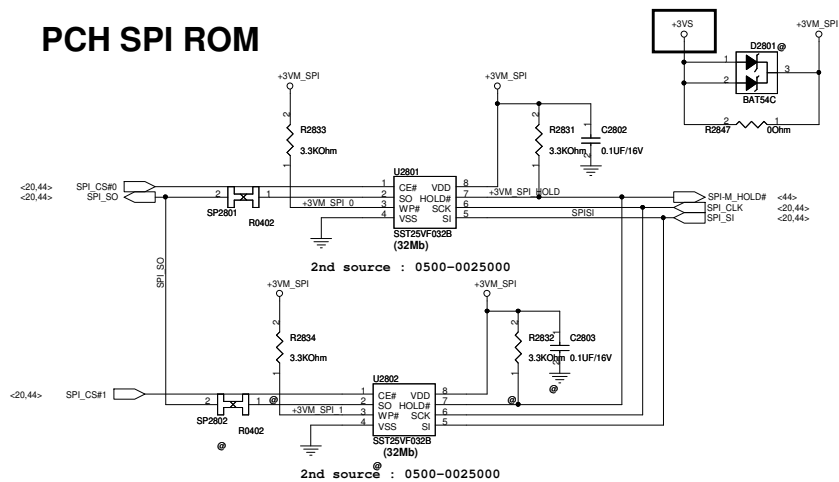


R1.4--1 08'WW50 MoW

+3VSO --- +3VS <3,16,17,20,21,22,23,24,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+3VSUS --- +3VSUS <27,30,33,34,81,92>
+VTT_CPU --- +VTT_CPU <3,6,28,32,57,82>
+3VSUS_ORG --- +3VSUS_ORG <21,22,24,27>



PCH SPI ROM

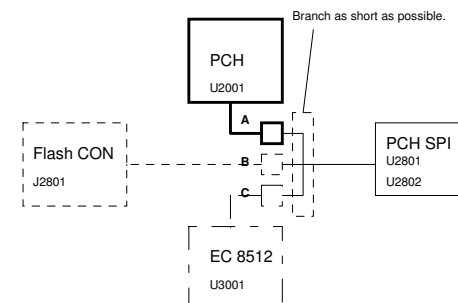


SPI FROM EC

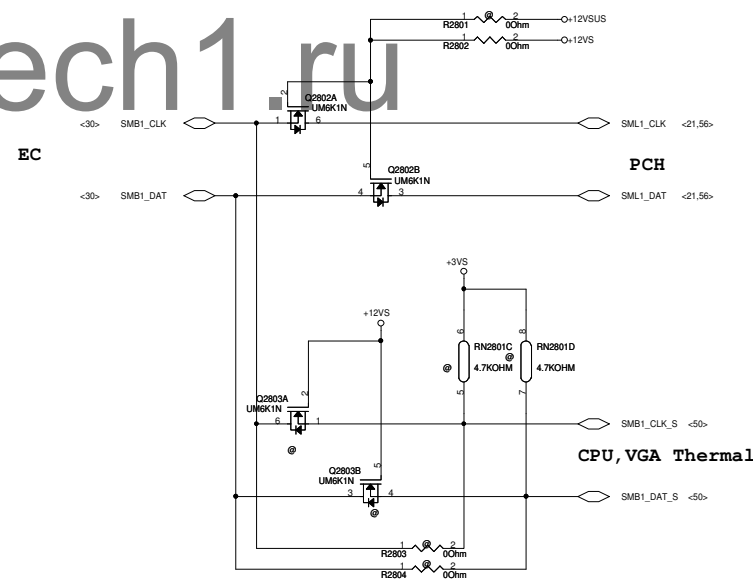
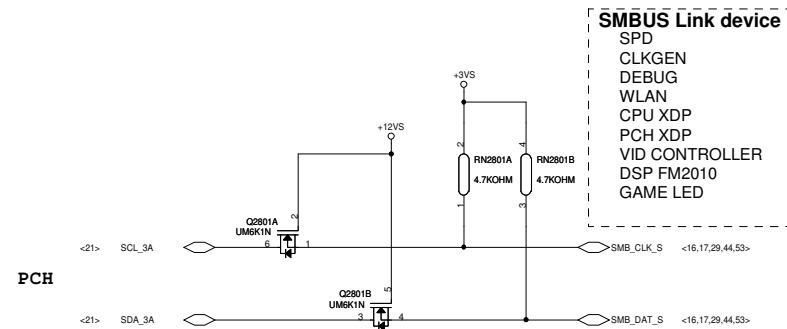
For EC request.

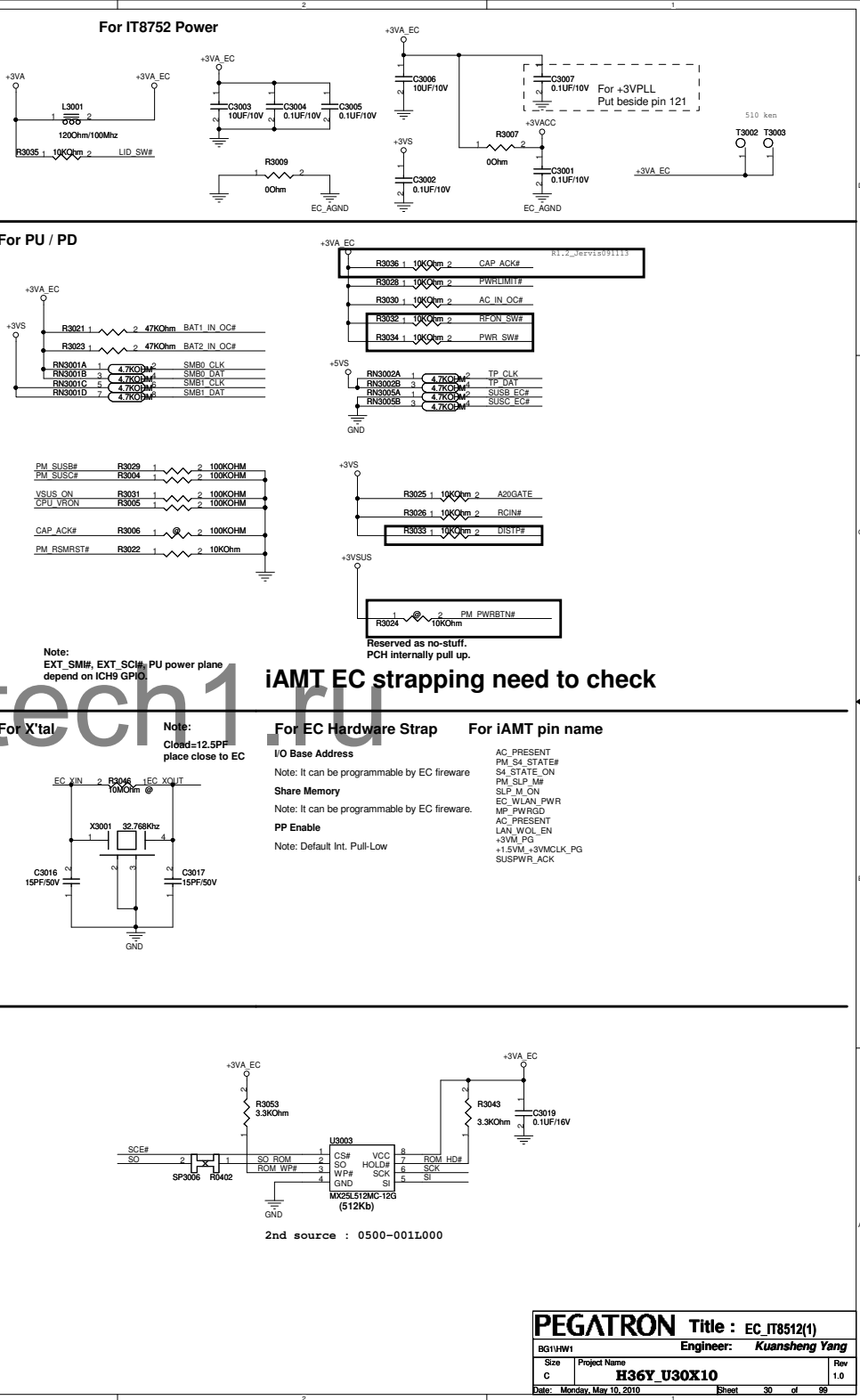
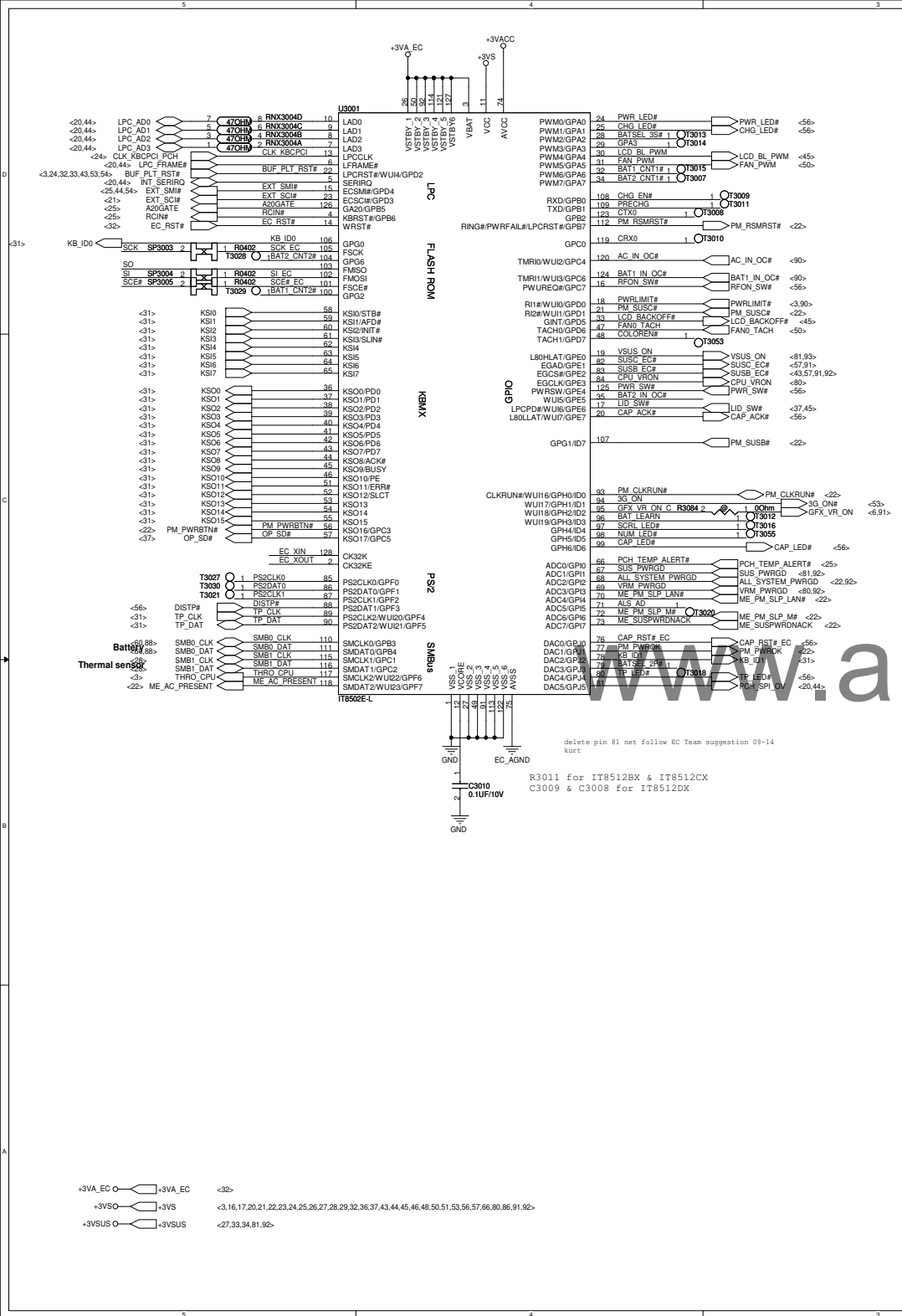
SPI FLASH CON

SPI Setting for layout:

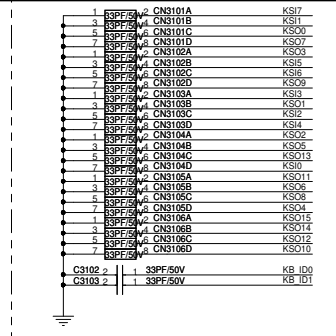
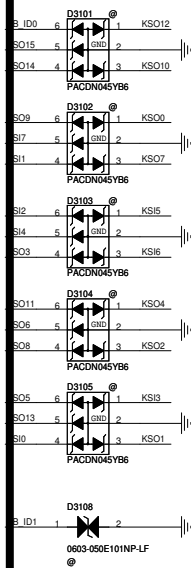


+3VSO	3V3	<3,16,17,20,21,22,23,24,25,26,27,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+12VS	12VS	<45,48,91>
+12VSUS	12VSUS	<81,91>
+3VM_SPI	3VM_SPI	<20,44>

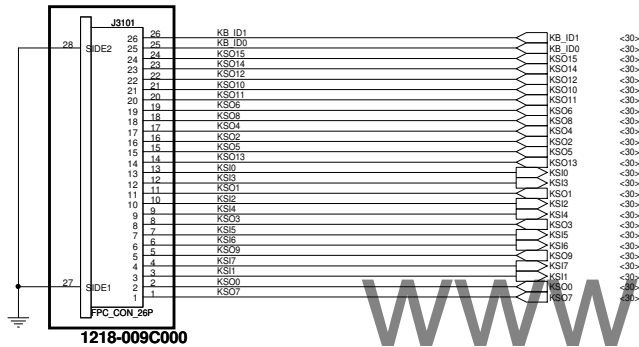




EMI

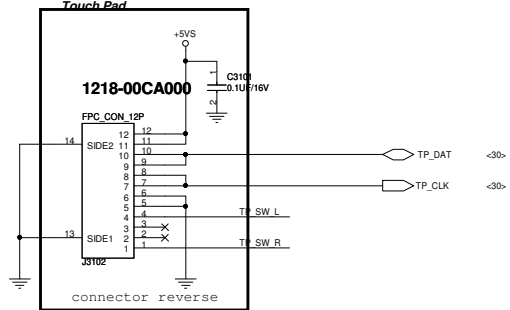


Keyboard

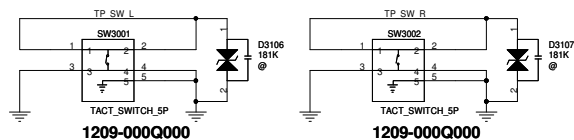


1218-009C000

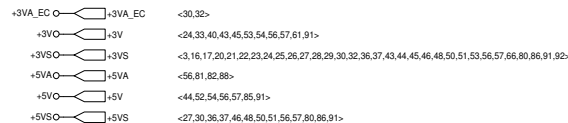
Touch Pad



1218-00CA000

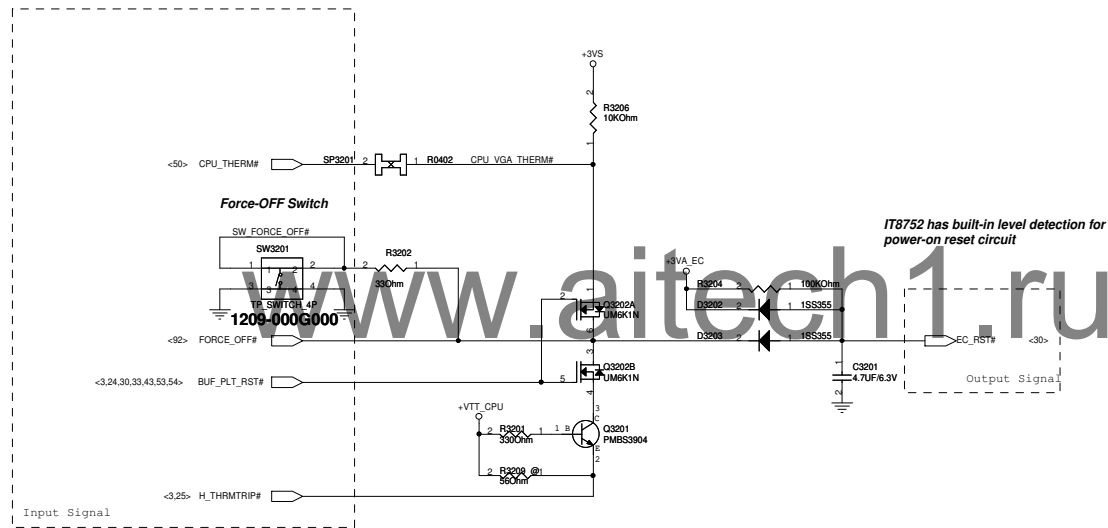


1209-000Q000

1st source: 1209-000P000
2nd source: 1209-000Q000

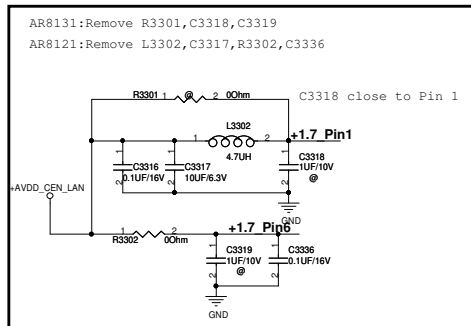
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Thermal Policy



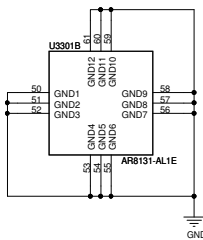
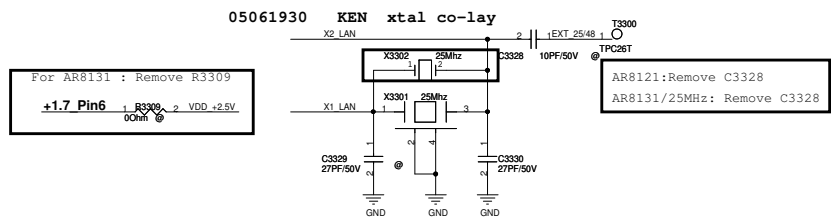
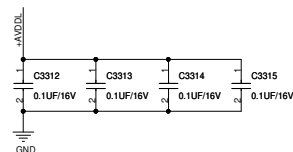
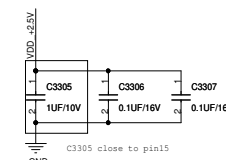
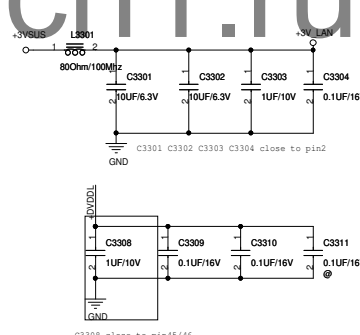
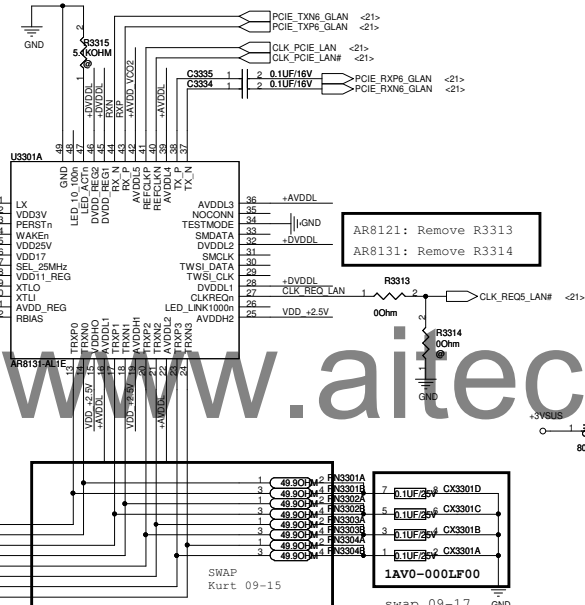
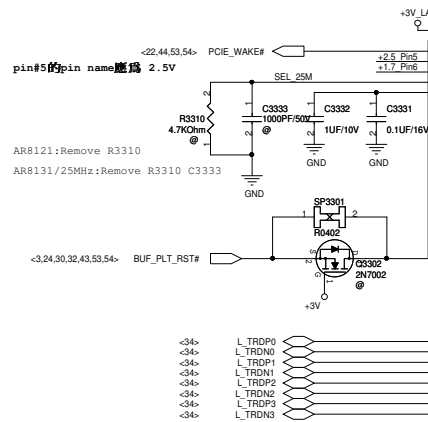
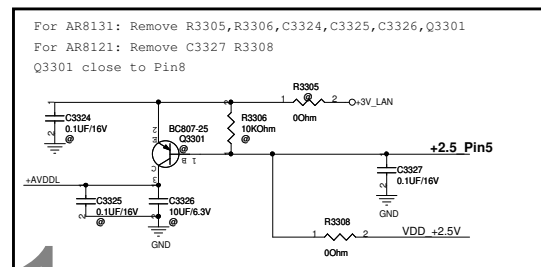
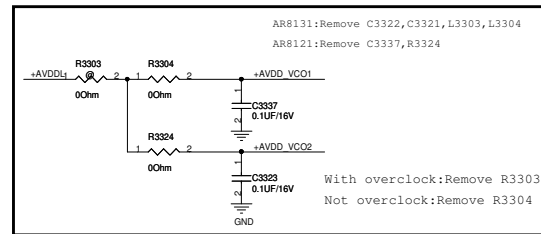
+VTT_CPU O — +VTT_CPU <3,6,25,26,57,82>
+3VA_EC O — +3VA_EC <30>
+3VSC O — +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

+3VS0 -> +3VS
 +3VS1 -> +3VSUS
 <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
 <27,30,34,81,92>

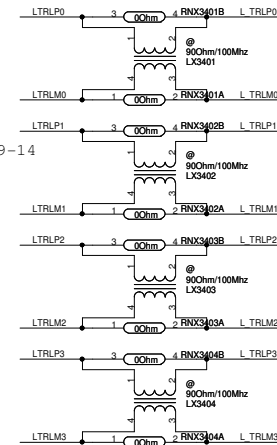
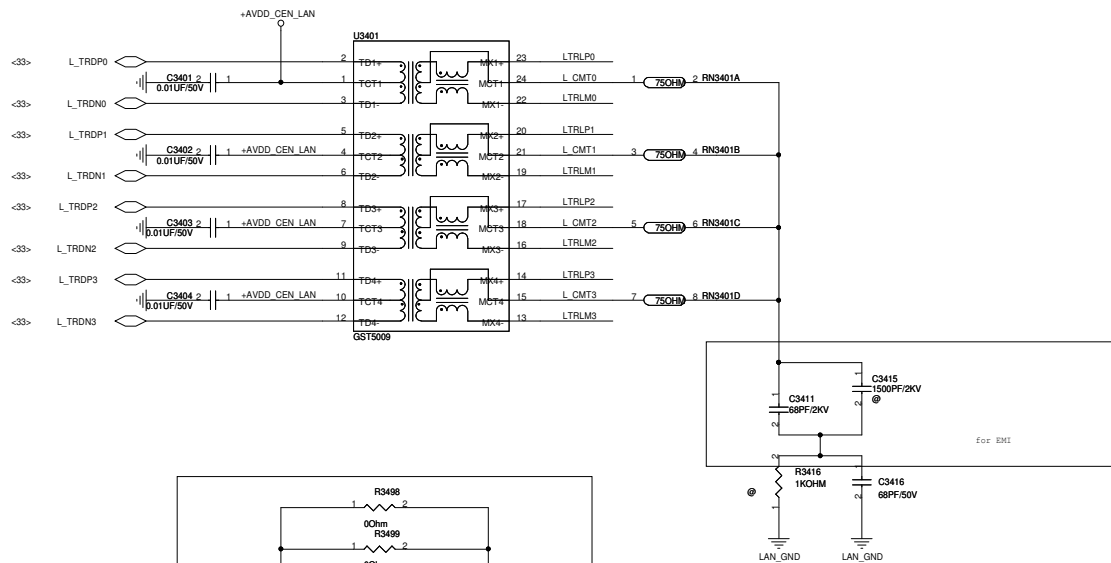


AR8131 with overclock: Remove R3315
 AR8121: Remove R3315

ground pad要打敷熱孔

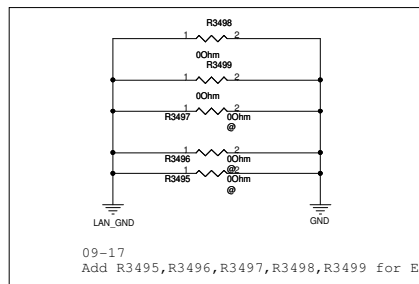


R1.4--6

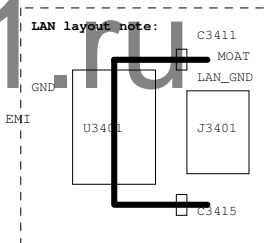
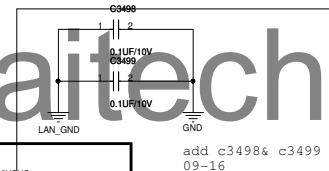


swap 09-14
kurt

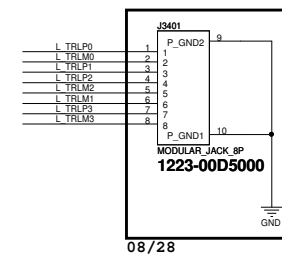
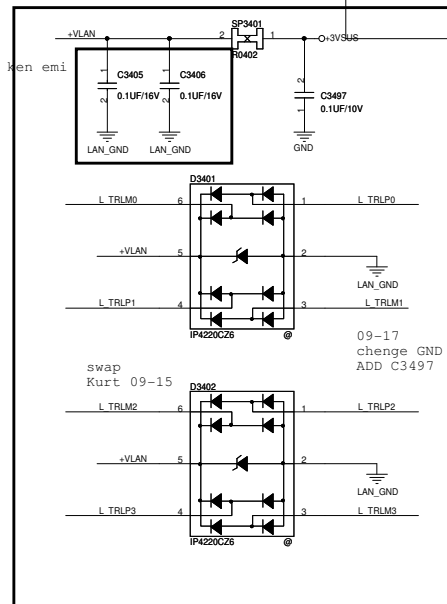
R1.4-2



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105101000 hen emi

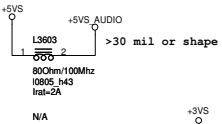
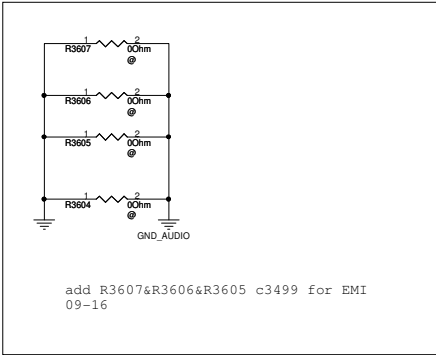
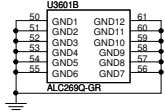
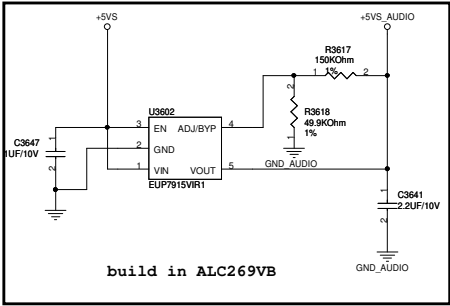


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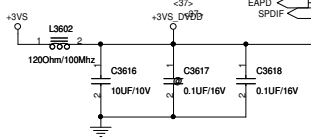
PEGATRON		Title : MDC CONN	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	35 of 99

DIGITAL ANALOG

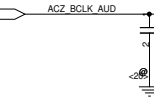
$V_{out} = 1.215 * (1 + (150K/49.9K)) = 4.86V$



SPDIF OUT

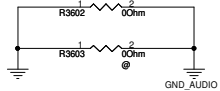


ACZ_BCLK_AUD



HP Jack Detect
EXT MIC Detect

INT MIC IN



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HeadPhone Out

EXT MIC Vref.
INT MIC Vref.

KEN 100324

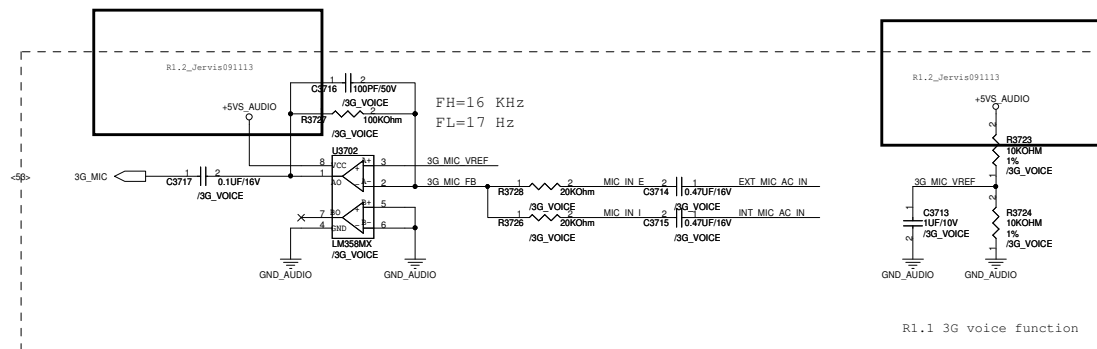
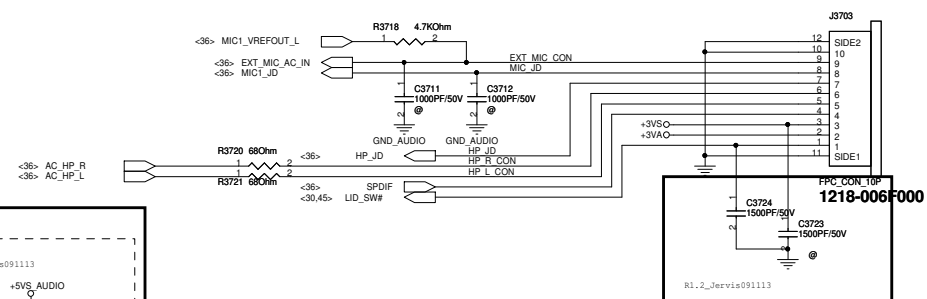
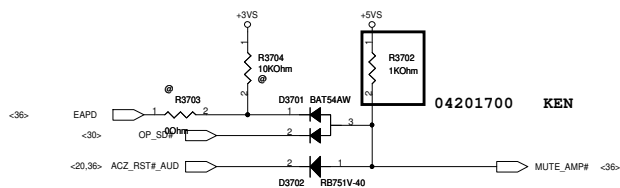
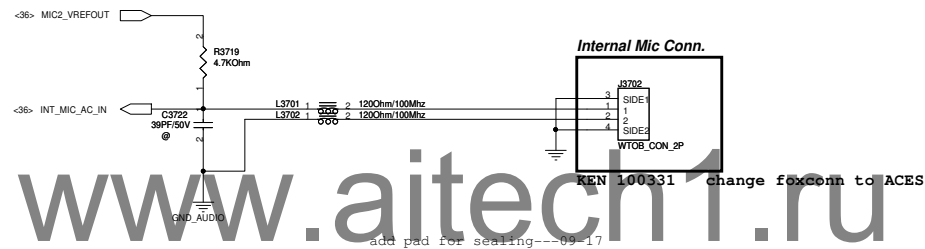
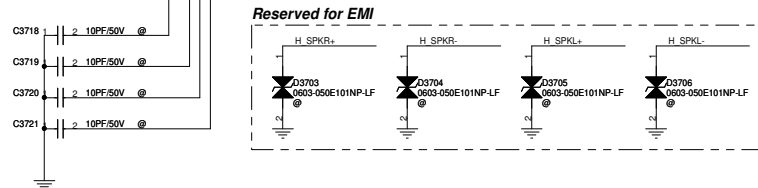
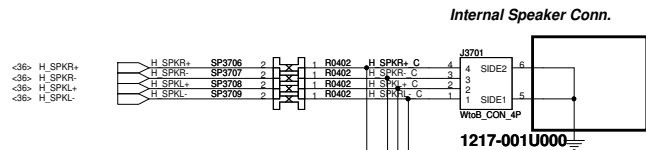
EXT MIC IN

PEGATRON Title : AUD(1).ALC269

BG1VHW1 Engineer: Kuansheng Yang

Size Project Name H36Y_U30X10 Rev 1.0

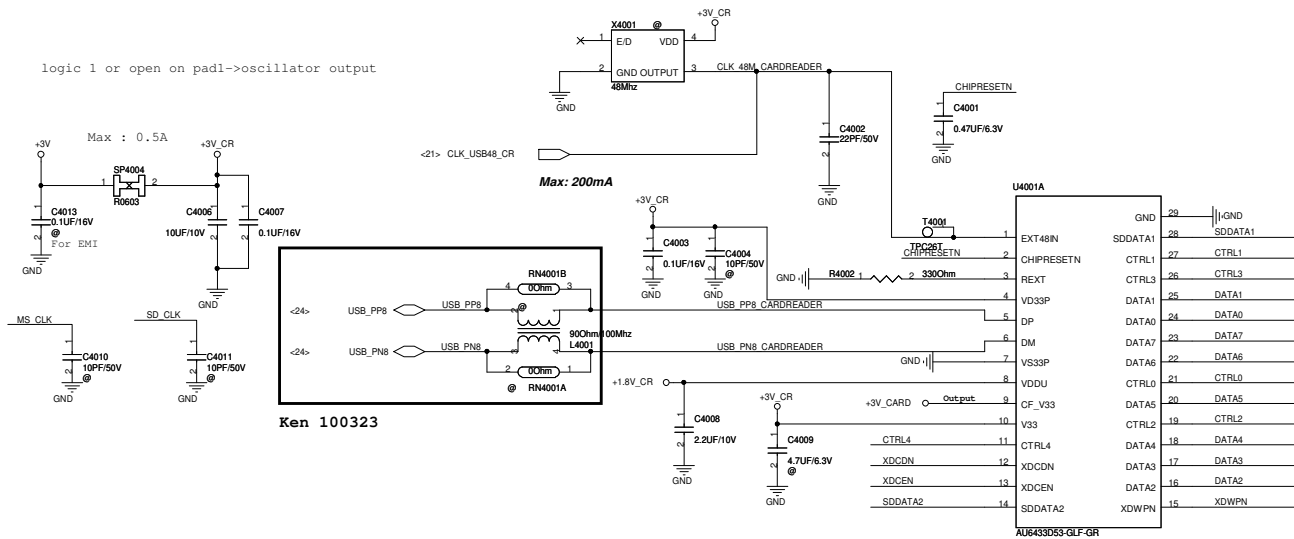
Date: Monday, May 10, 2010 Sheet 36 of 99



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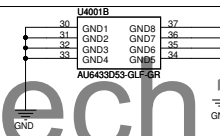
www.aitech1.ru

PEGATRON		Title : AUD(4) ****	
BG1HW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
Custom	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	39 of 99

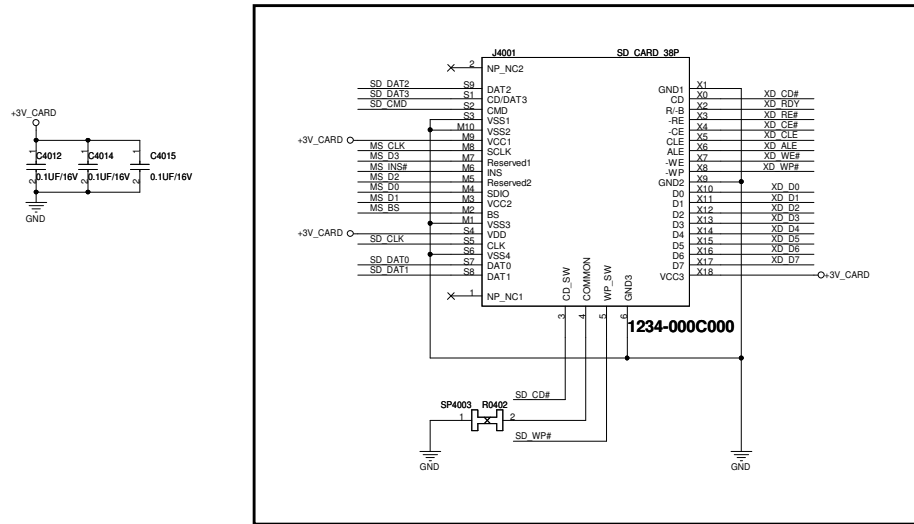


Pin Name	Description
CTRL4	XDRDN/ MSINS
XDCDN	XDCDN
XDCEN	XDCEN
SDDATA2	SDDATA2
XDWPN	XDWPN
DATA2	XDDATA2/ MSDATA2
DATA3	SDDATA3/ XDDATA3/ MSDATA3
DATA4	SDDATA4/ XDDATA4/ MSDATA4
CTRL2	SDCMD/ XDRBN
DATA5	SDDATA5/ XDDATA5/ MSDATA5
CTRL0	SDCLK/ XDALE/ MSBS
DATA6	SDDATA6/ XDDATA6/ MSDATA6
DATA7	SDDATA7/ XDDATA7/ MSDATA7
DATA0	SDDATA0/ XDDATA0/ MSDATA0
DATA1	XDDATA1/ MSDATA1
CTRL3	SDCDN/ XDWPN
CTRL1	SDWP/ XDCLE/ MSCLK
SDDATA1	SDDATA1

CTRL4	XD RE#	MS INS#
XDCDN	XD CD#	
XDCEN	XD CE#	
SDDATA2	SD DAT2	
XDWPN	XD WP#	MS D2
DATA2	SD DAT3	MS D3
DATA3	SD DAT4	MS D4
DATA4	SD CMD	MS D5
CTRL2	SD CLK	MS BS
DATA5	SD DAT5	MS D6
CTRL0	SD CLK	MS D7
DATA6	SD DAT6	MS D8
DATA7	SD DAT7	MS D9
DATA0	SD DAT0	MS D10
DATA1	SD CD#	MS D1
CTRL3	SD WP#	MS WE#
SDDATA1	SD DAT1	MS CLK



add thermal pad --11-12

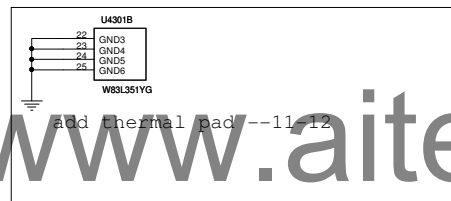
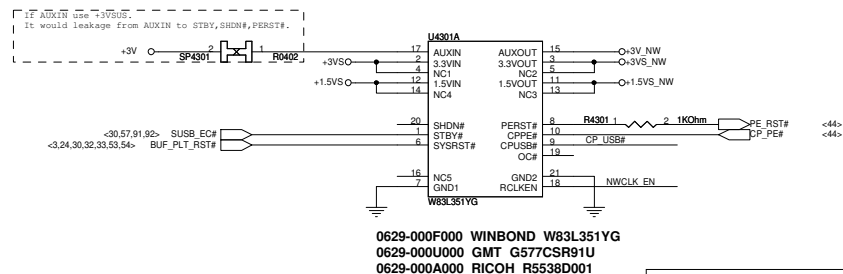
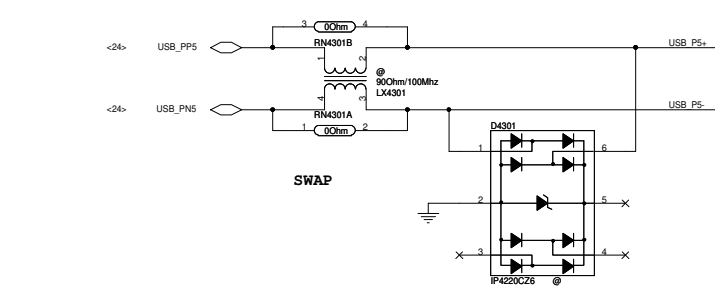


+3V5O—+3V5 <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>

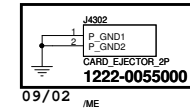
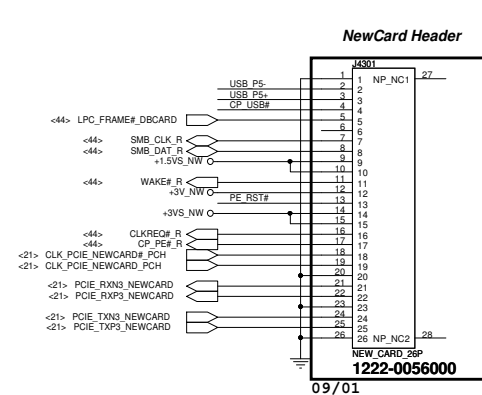
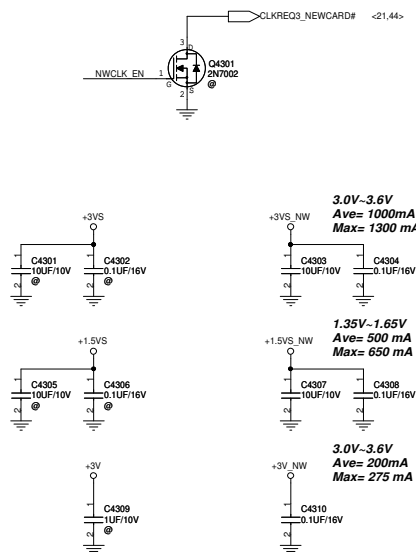
www.aitech1.ru

+3VSO — +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+12VO — +12V <91>

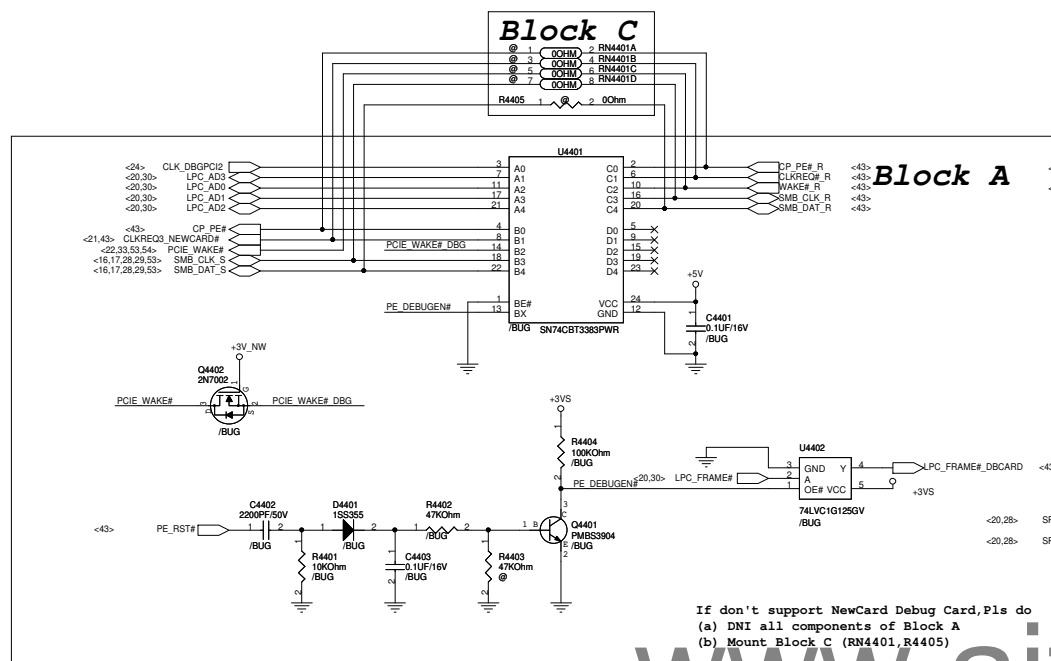
www.aitech1.ru



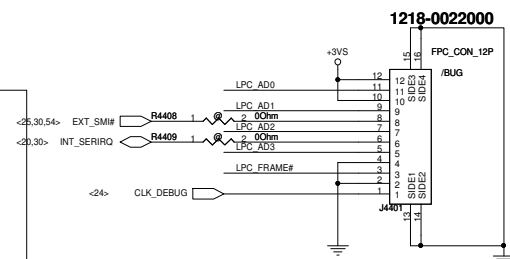
+1.5VS ○ 1.5VS <26,53,57,91>
+3V ○ 3V <24,33,40,45,53,54,56,57,61,91>
+3VS ○ 3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,44,45,46,48,50,51,53,56,57,66,80,86,91,92>



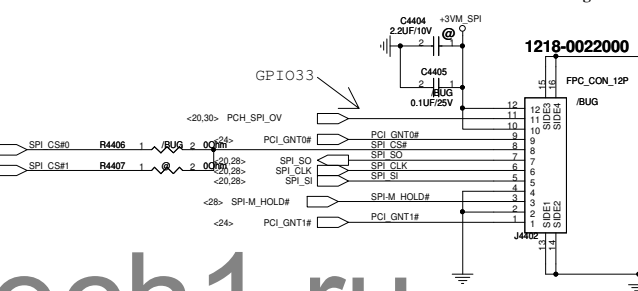
For NewCard Debug Card



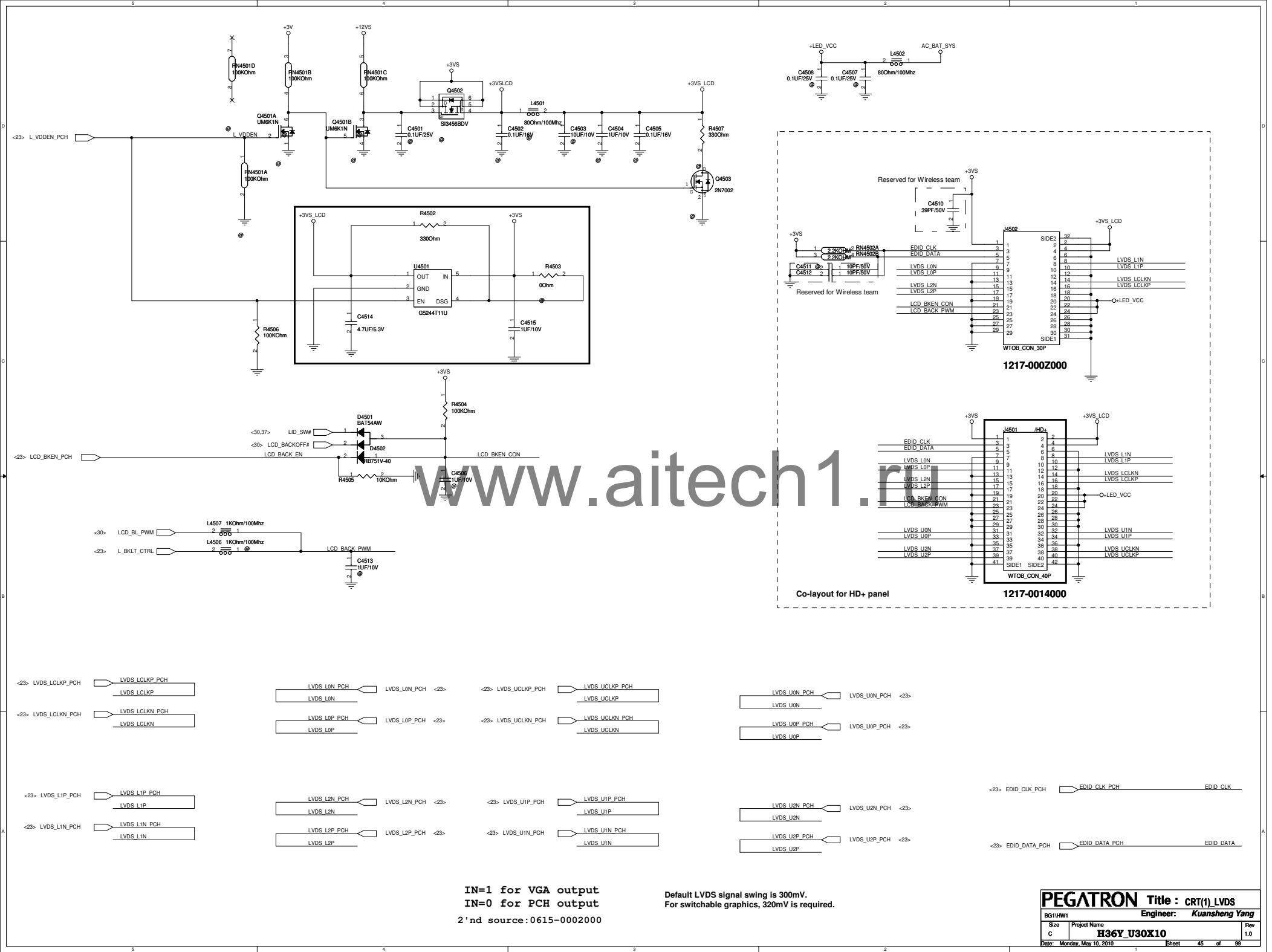
LPC Debug Port

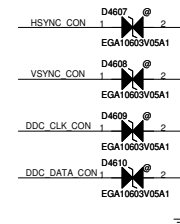
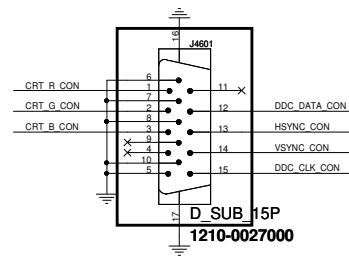
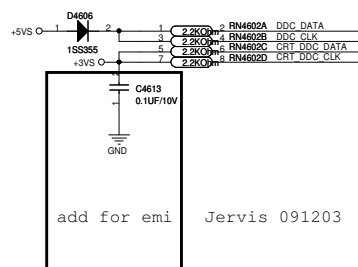
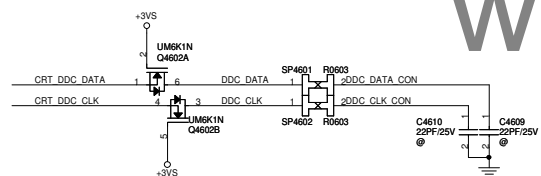
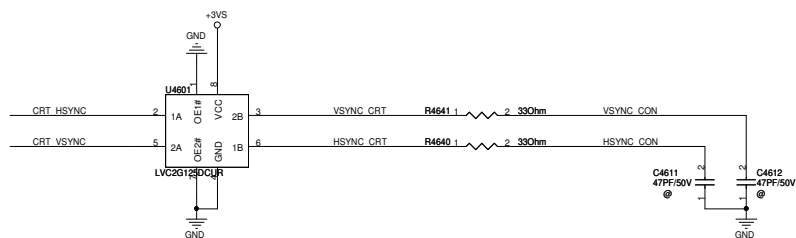
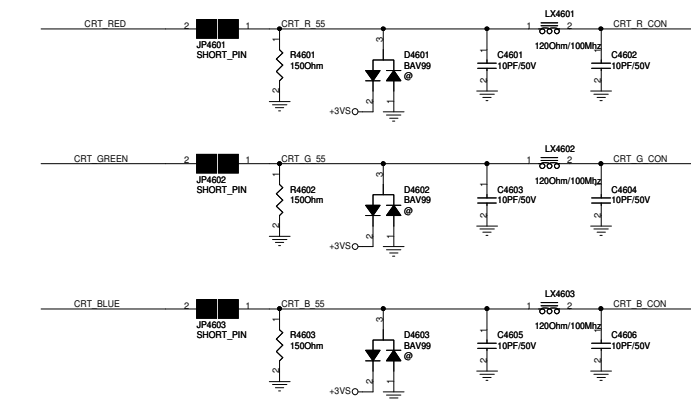


SPI Connector Debug Connector



+5VCO — 5V <52,54,56,57,85,91>
+3VCO — 3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,45,46,48,50,51,53,56,57,66,80,86,91,92>





<23> CRT_R_PCH CRT RED
<23> CRT_G_PCH CRT GREEN
<23> CRT_B_PCH CRT BLUE

<23> CRT_HSYNC_PCH CRT HSYNC
<23> CRT_VSYNC_PCH CRT VSYNC

<23> DDC_DATA_PCH CRT DDC DATA
<23> DDC_CLK_PCH CRT DDC CLK

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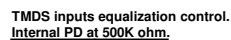
+3VS -> +3VS
+5VS -> +5V
+5VS -> +5VS

<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,48,50,51,53,56,57,66,80,86,91,92>
<44,52,54,56,57,85,91>
<27,30,31,36,37,48,50,51,56,57,80,86,91>

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R2.0

+3VSO +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,86,91,92>
+5VSO +5VS <27,30,31,36,37,46,48,50,51,56,57,80,86,91>

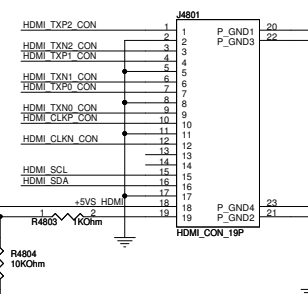
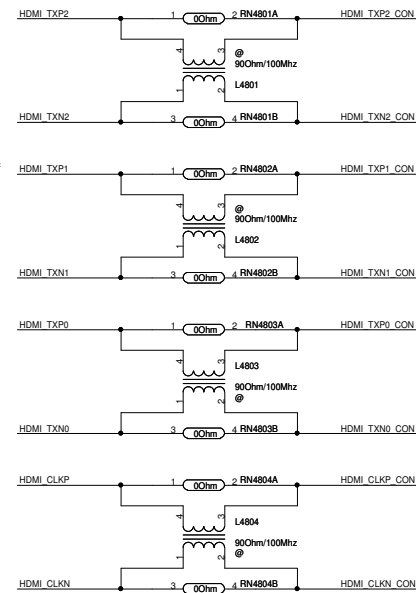
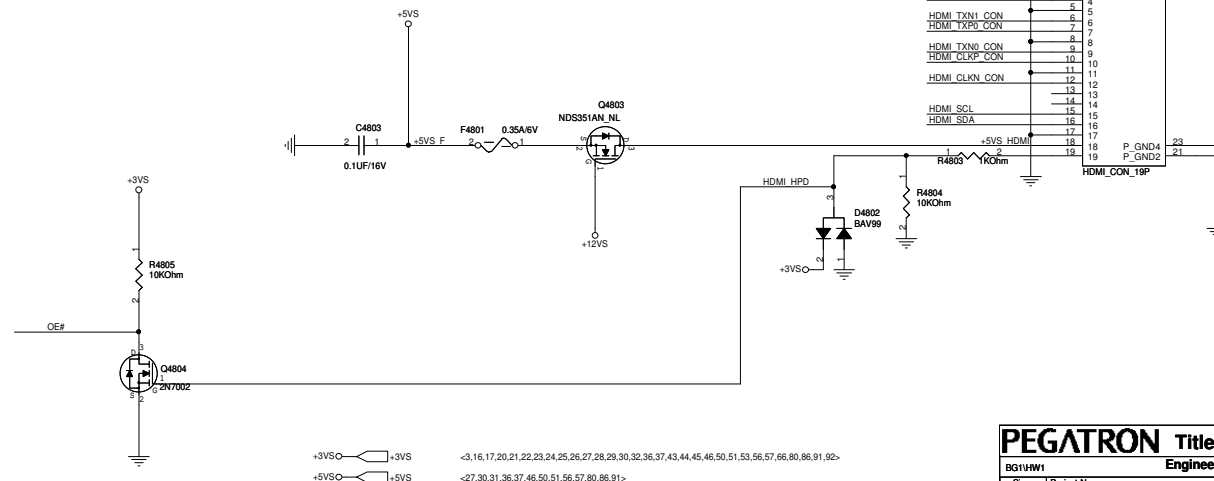


PC1	PC0	
0	0	8dB
0	1	4dB
1	0	12dB
1	1	0dB

HPD# output voltage configuration

CFG1 CFG0	Voh of HDP#
0 0	0.9V
0 1	0.8V
1 0	1.0V
1 1	External pull-up resistor, Voh is determined by external supply.

External pull-up resistor,
Voh is determined by external supply

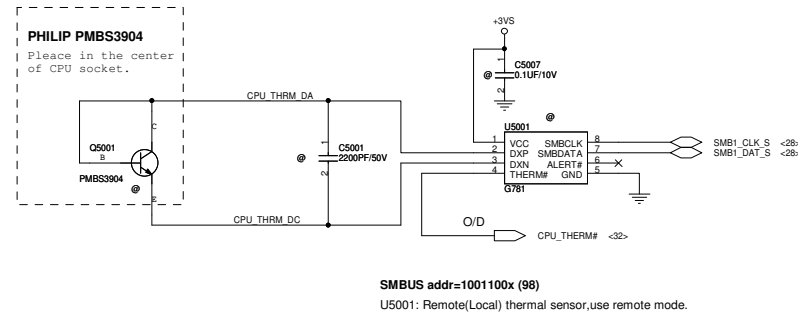


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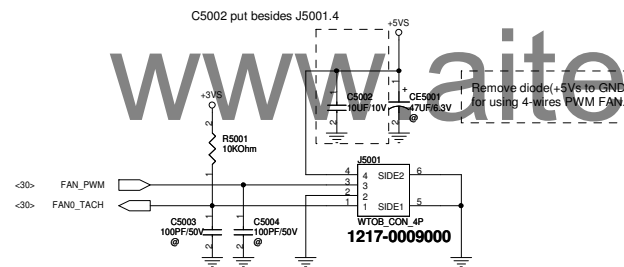
PEGATRON		Title : TV(2) ****	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	49 of 99

+3VS ———— +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,51,53,56,57,66,80,86,91,92>
+5VS ———— +5VS <27,30,31,36,37,46,48,51,56,57,80,86,91>

CPU Thermal Sensor

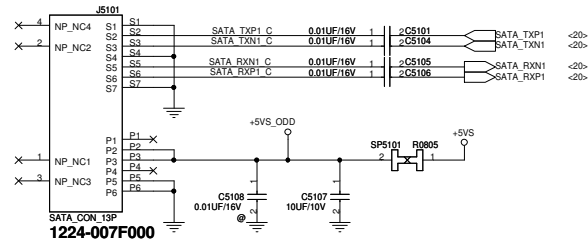


PWM Fan



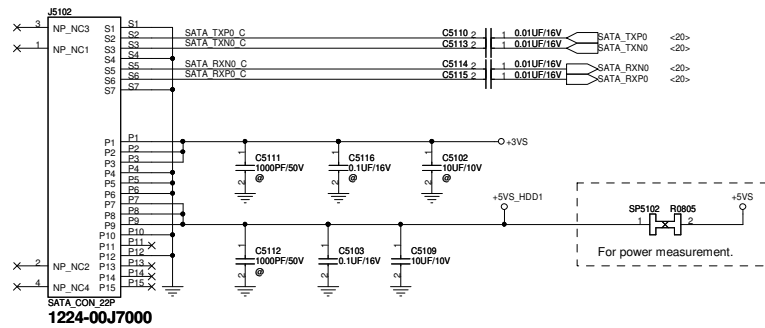
ODD

+3VS \rightarrow +3VS <3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,53,56,57,66,80,86,91,92>
+5VS \rightarrow +5VS <27,30,31,36,37,46,48,50,56,57,80,86,91>

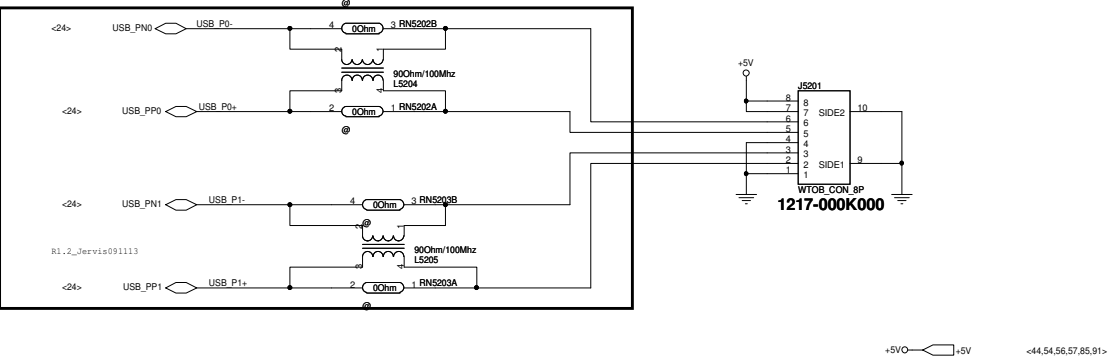


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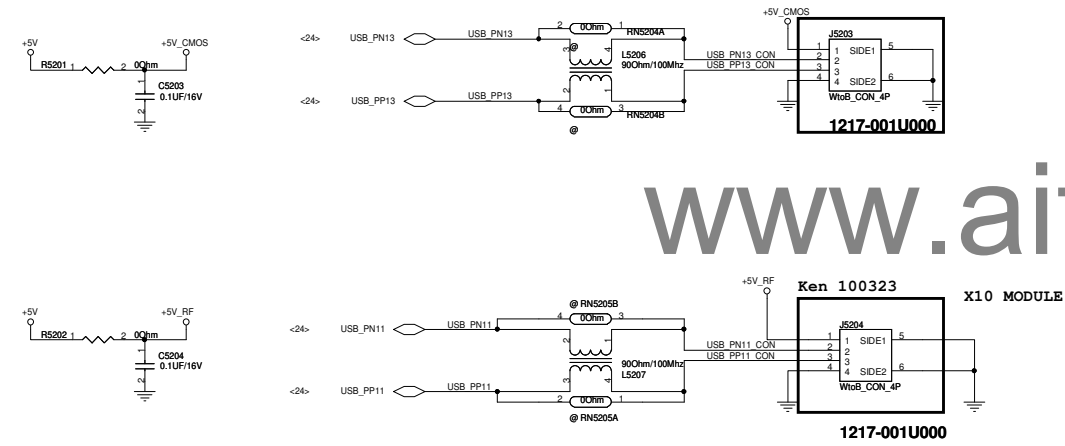
HDD

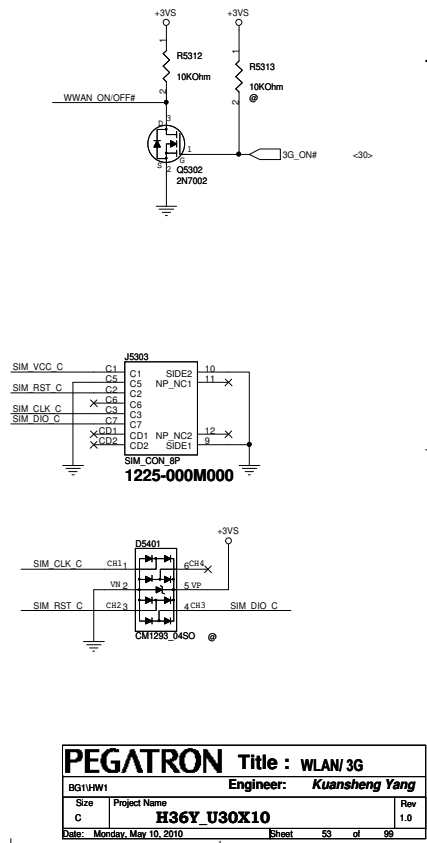
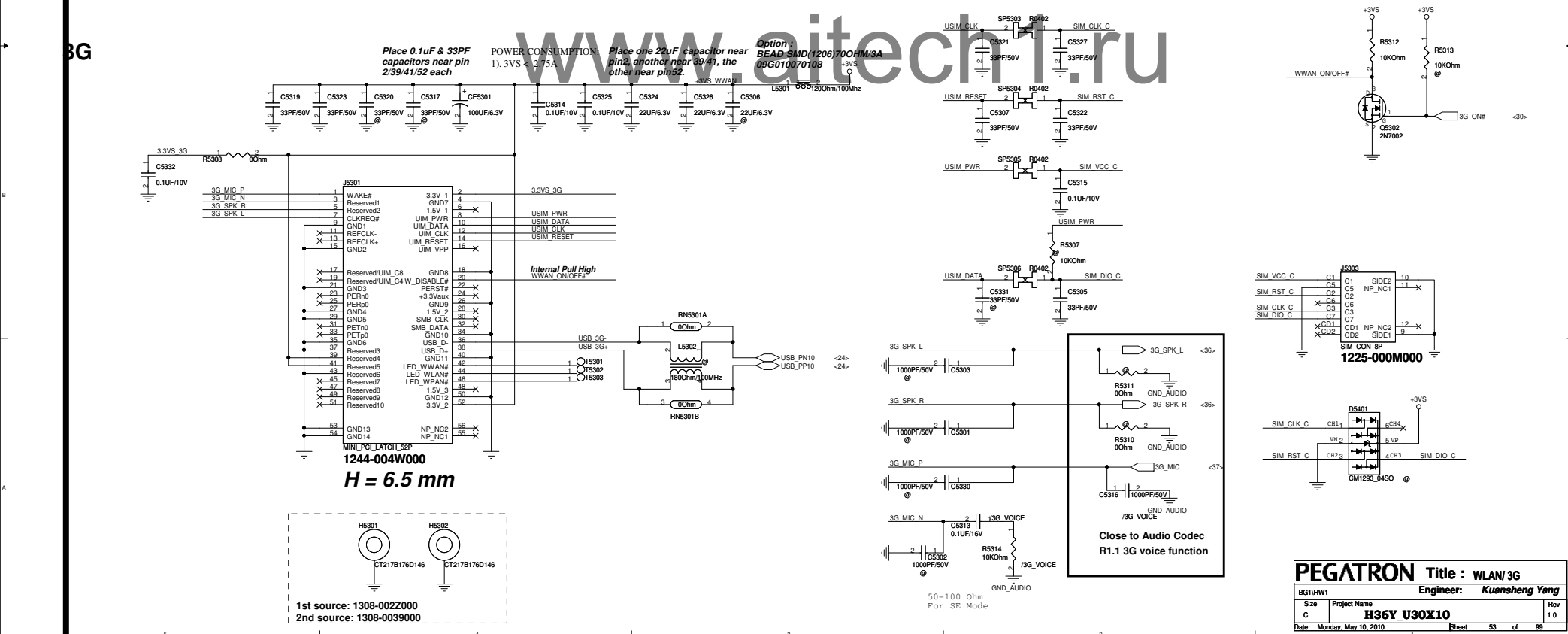


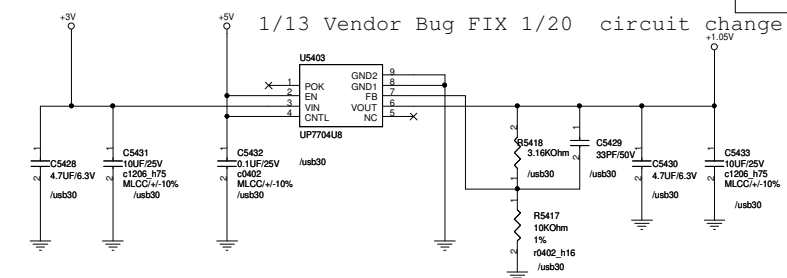
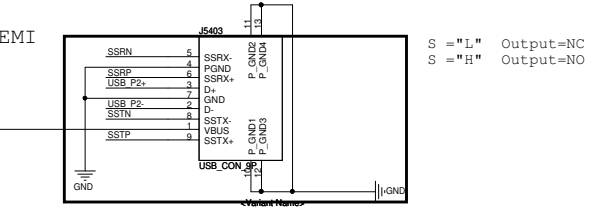
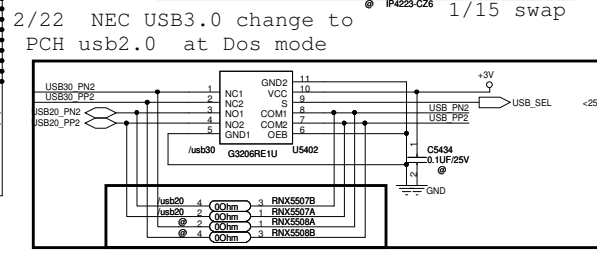
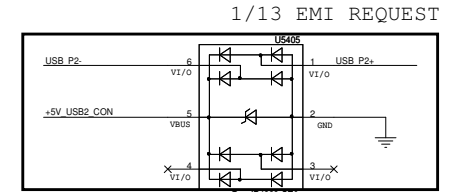
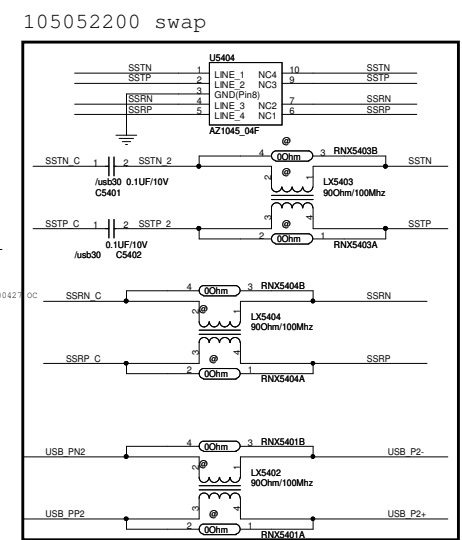
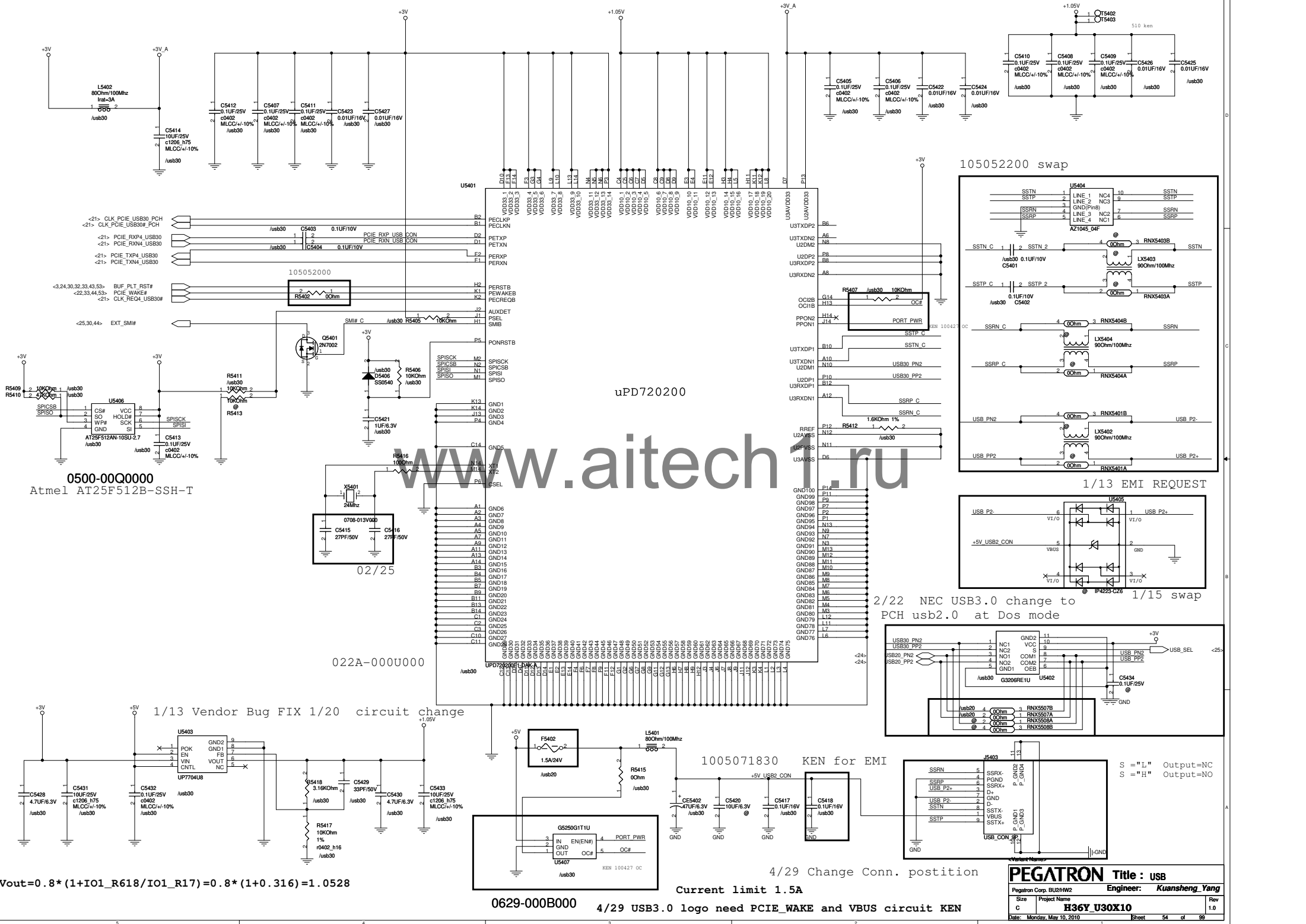
USB ports



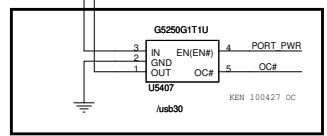
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BG



$$V_{out} = 0.8 * (1 + I_{O1_R618} / I_{O1_R17}) = 0.8 * (1 + 0.316) = 1.0528$$



Current limit 1.5A

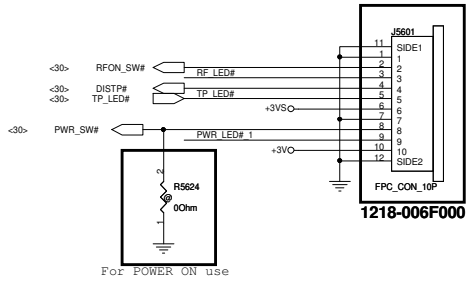
0629-000B000

4/29 USB3.0 logo need PCIE_WAKE and VBUS circuit KEN

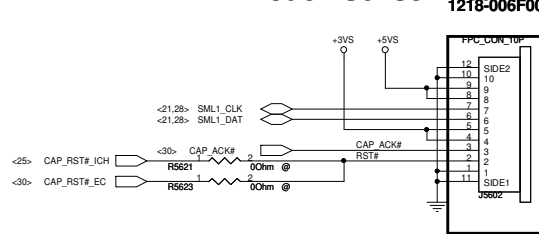
4/29 Change Conn. postition

PEGATRON Title : USB			
Pegatron Corp. BU21HW2		Engineer: Kuansheng Yang	
Size C	Project Name	H36Y_U30X10	Rev 1.0
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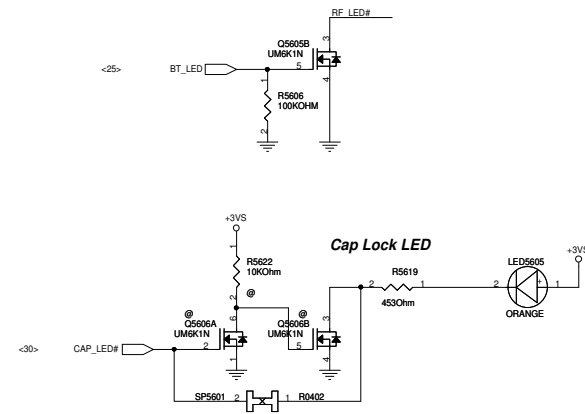
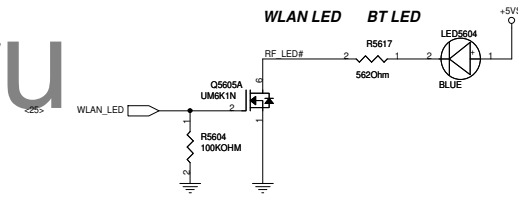
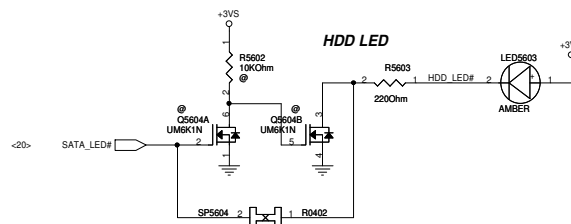
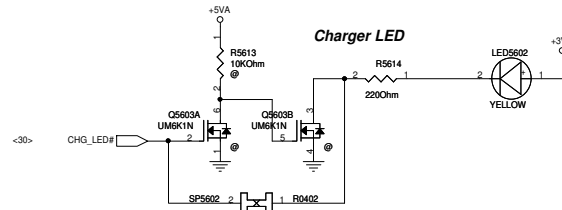
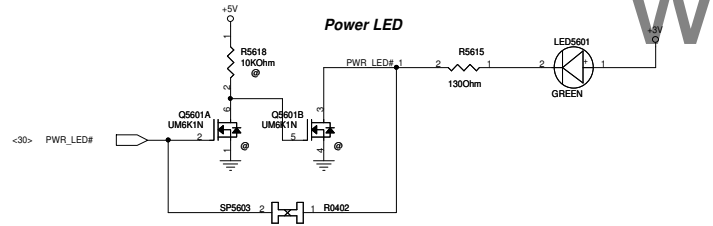
Power Switch Board Conn



Touch Sensor Board Conn

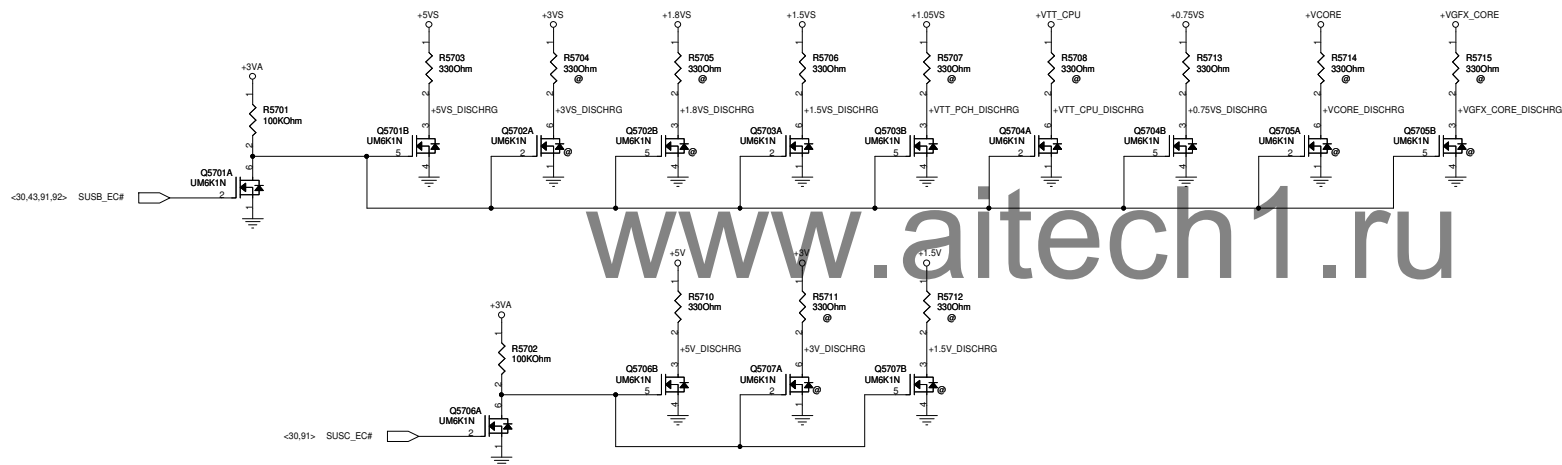


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+3VAC	+3VA	<20,30,37,57,81,93>
+3VS	+3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,57,66,80,86,91,92>
+5VSUS	+5VSUS	<27,81,91>
+5VAC	+5VA	<81,82,88>
+5VS	+5V	<44,52,54,57,85,91>
+5VS	+5VS	<27,30,31,36,37,46,48,50,51,57,80,86,91>
AC_BAT_SYS	AC_BAT_SYS	<45,80,81,82,83,86,88>

+3VA	3VA	<20,30,37,56,81,93>
+VOCORE	VOCORE	<6,80>
+VGFX_CORE	VGFX_CORE	<6,86,91>
+VTT_CPU	VTT_CPU	<3,6,25,26,32,82>
+0.75VS	0.75VS	<16,17,83>
+1.05VS	1.05VS	<26,27,29,80,82>
+1.5VS	1.5VS	<26,43,53,91>
+1.8VS	1.8VS	<6,26,85>
+3VS	3VS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,66,80,86,91,92>
+5VS	5VS	<27,30,31,36,37,46,48,50,51,53,56,80,86,91>
+1.5V	1.5V	<3,6,16,83>
+3V	3V	<24,33,40,43,45,53,54,56,61,91>
+5V	5V	<44,52,54,56,85,91>



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PEGATRON		Title : PCI ****	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
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PEGATRON		Title : DJ_****	
BG1VHW1		Engineer: Kuansheng Yang	
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Current setting=6A
Depend on the current of the adaptor.

5V_DVDD

510 ken

J6001

WTR06_CON_IP

1217-0037000

5V

0.1UF/25V

D6001 SS0540

L6001 1 2 800nH/100MHz

L6006 1 2 800nH/100MHz

C6002 10UF/25V

C6003 1UF/25V



















C6004 0.1UF/25V


















































C6005 0.1UF/25V

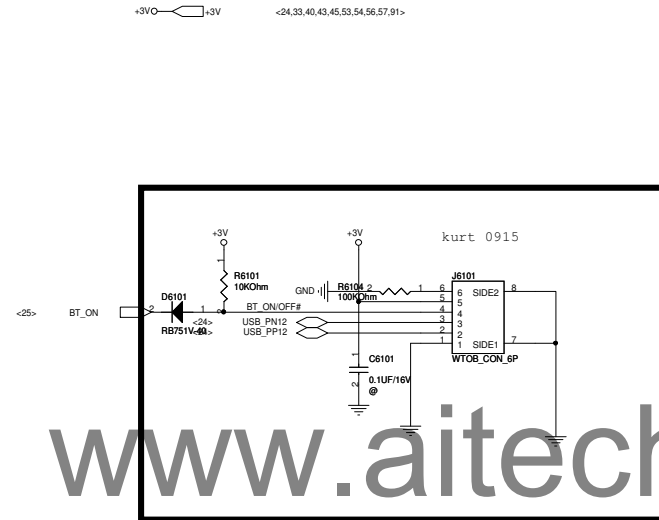
A/D_DOCK_IN

GND

[illegible]

+VCC_RTC		+VCC_RTC	<20,27>
+3VA_EC		+3VA_EC	<30,32>
+3VAO		+3VA	<20,30,37,56,57,81,93>
+5VAO		+5VA	<56,81,82,88>
+3VSUS		+3VSUS	<27,30,33,34,81,92>
+5VSUS		+5VSUS	<27,81,91>
+12VSUS		+12VSUS	<28,81,91>
+1.5V		+1.5V	<3,6,16,57,83>
+3VO		+3V	<24,33,40,43,45,53,54,56,57,81,91>
+5VO		+5V	<44,52,54,56,57,85,91>
+12V		+12V	<91>
+0.7VSUS		+0.7VSUS	<16,17,57,83>
+1.05VSUS		+1.05VSUS	<26,27,29,57,80,82>
+1.5VSUS		+1.5VSUS	<26,43,53,57,91>
+1.8VSUS		+1.8VSUS	<6,26,57,85>
+3VSUS		+3VSUS	<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,66,80,81,92>
+5VSUS		+5VSUS	<27,30,31,36,37,46,48,50,51,56,57,80,86,91>
+12VSUS		+12VSUS	<28,45,48,91>

AC_BAT_SYS		AC_BAT_SYS	<45,80,81,82,83,86,88>
A/D_DOCK_IN		A/D_DOCK_IN	<88>
BAT_CON		BAT_CON	<88>
+1.5V_DDR3		+1.5V_DDR3	<16,17,18>
+VTT_CPU		+VTT_CPU	<3,25,26,32,57,82>
+VCORE		+VCORE	<65,87,80>
+VGFX_CORE		+VGFX_CORE	<65,86,89,1>
+VTT_PCH_ORG		+VTT_PCH_ORG	<21,22,26,27>
+VTT_PCH_VCCIO		+VTT_PCH_VCCIO	<20,26,27>
+1.05MV_ORG		+1.05MV_ORG	<27>
+V_NVRAM_VCCQ		+V_NVRAM_VCCQ	<26>
+VREFD_DIMM0		+VREFD_DIMM0	<18,18>
+VREFD_DIMM1		+VREFD_DIMM1	<18,18>
+VREFD_DIMM2		+VREFD_DIMM2	<17,18>
+VREFD_DIMM3		+VREFD_DIMM3	<17,18>
+VREFD_DIMM4		+VREFD_DIMM4	<17,18>
+VREFD_DIMM5		+VREFD_DIMM5	<17,18>
+VREFD_DIMM6		+VREFD_DIMM6	<17,18>
+VREFD_DIMM7		+VREFD_DIMM7	<17,18>
+VREFD_DIMM8		+VREFD_DIMM8	<17,18>
+VREFD_DIMM9		+VREFD_DIMM9	<17,18>
+VREFD_DIMM10		+VREFD_DIMM10	<17,18>
+VREFD_DIMM11		+VREFD_DIMM11	<17,18>
+VREFD_DIMM12		+VREFD_DIMM12	<17,18>
+VREFD_DIMM13		+VREFD_DIMM13	<17,18>
+VREFD_DIMM14		+VREFD_DIMM14	<17,18>
+VREFD_DIMM15		+VREFD_DIMM15	<17,18>
+VREFD_DIMM16		+VREFD_DIMM16	<17,18>
+VREFD_DIMM17		+VREFD_DIMM17	<17,18>
+VREFD_DIMM18		+VREFD_DIMM18	<17,18>
+VREFD_DIMM19		+VREFD_DIMM19	<17,18>
+VREFD_DIMM20		+VREFD_DIMM20	<17,18>
+VREFD_DIMM21		+VREFD_DIMM21	<17,18>
+VREFD_DIMM22		+VREFD_DIMM22	<17,18>
+VREFD_DIMM23		+VREFD_DIMM23	<17,18>
+VREFD_DIMM24		+VREFD_DIMM24	<17,18>
+VREFD_DIMM25		+VREFD_DIMM25	<17,18>
+VREFD_DIMM26		+VREFD_DIMM26	<17,18>
+VREFD_DIMM27		+VREFD_DIMM27	<17,18>
+VREFD_DIMM28		+VREFD_DIMM28	<17,18>
+VREFD_DIMM29		+VREFD_DIMM29	<17,18>
+VREFD_DIMM30		+VREFD_DIMM30	<17,18>
+VREFD_DIMM31		+VREFD_DIMM31	<17,18>
+VREFD_DIMM32		+VREFD_DIMM32	<17,18>
+VREFD_DIMM33		+VREFD_DIMM33	<17,18>
+VREFD_DIMM34		+VREFD_DIMM34	<17,18>
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+VREFD_DIMM37		+VREFD_DIMM37	<17,18>



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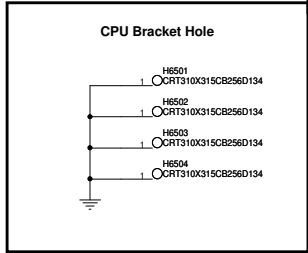
PEGATRON		Title : TPM_****	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	62 of 99

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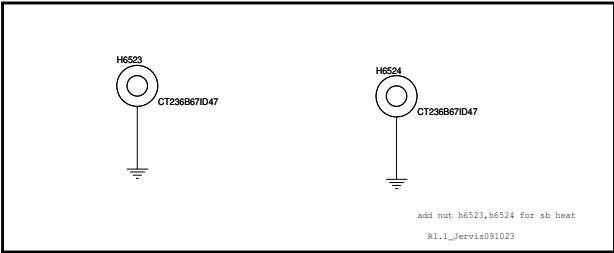
PEGATRON		Title : N/A	
BG1VHW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y U30X10		1.0
Date: Monday, May 10, 2010		Sheet	63 of 99

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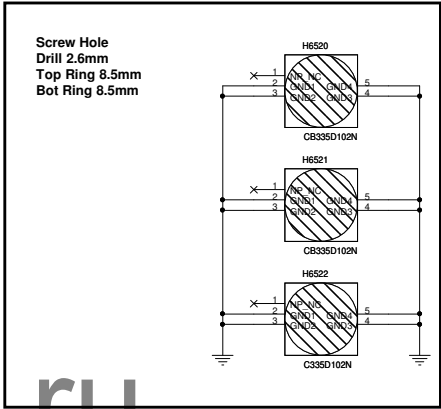
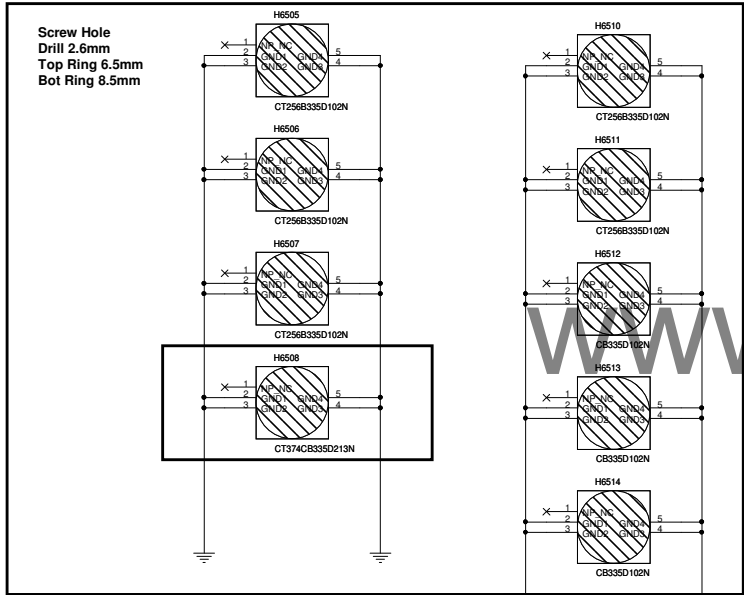
PEGATRON		Title : TUN_TV Tuner	
BG1VHW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	64 of 99



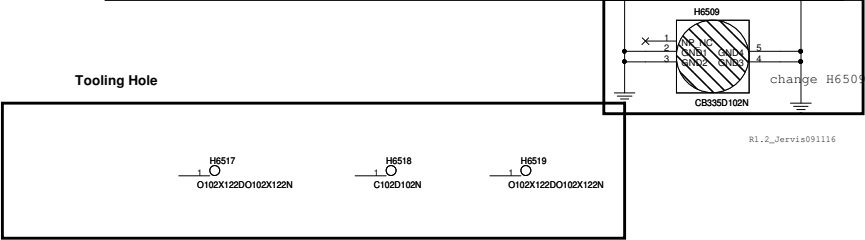
Change H6509 PARTNUMBER TO s04498
R1.1_Jervis091023



add nut h6523,h6524 for sb heat
R1.1_Jervis091023



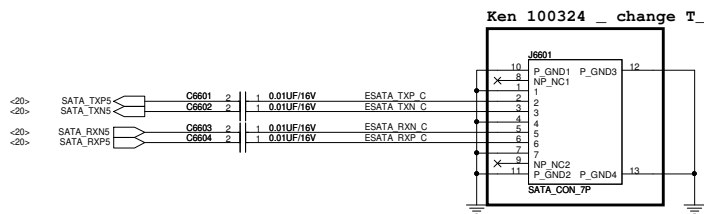
change H6512,H6513,H6514,H6520,H6521 partnumber to s04545
R1.1_Jervis091023



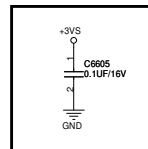
change H6509 partnumber to s04545

R1.2_Jervis091116

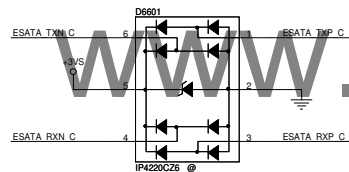
+3VS ○ ———] +3VS
+1.8VS ○ ———] +1.8VS
<3,16,17,20,21,22,23,24,25,26,27,28,29,30,32,36,37,43,44,45,46,48,50,51,53,56,57,80,86,91,92>
<6,26,57,85>



Ken 1005071830 for EMI



for EMI request,delete ESATA_GND
09-17



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PEGATRON		Title : ONFI	
BG1VHW1		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y U30X10		1.0
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PEGATRON		Title : N/A	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
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PEGATRON		Title : OTH	
BG1VHW1		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
Date: Monday, May 10, 2010		Sheet	69 of 99

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PEGATRON		Title : VGA Main (1)	
<OrgName>		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y_U30X10		1.0
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PEGATRON		Title : <Title>	
<OrgName>		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
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PEGATRON		Title : <Title>	
<OrgName>		Engineer: Kuansheng Yang	
Size	Project Name	Rev	
C	H36Y U30X10	1.0	
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PEGATRON		Title : POWER (1)	
PEGATRON		Engineer: Kuansheng Yang	
Size	Project Name	Rev	
Custom	H36Y_U30X10	1.0	
Date: Monday, May 10, 2010		Sheet	75 of 99

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PEGATRON		Title : POWER (2)	
<OrgName>		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y U30X10		1.0
Date: Monday, May 10, 2010		Sheet	76 of 99

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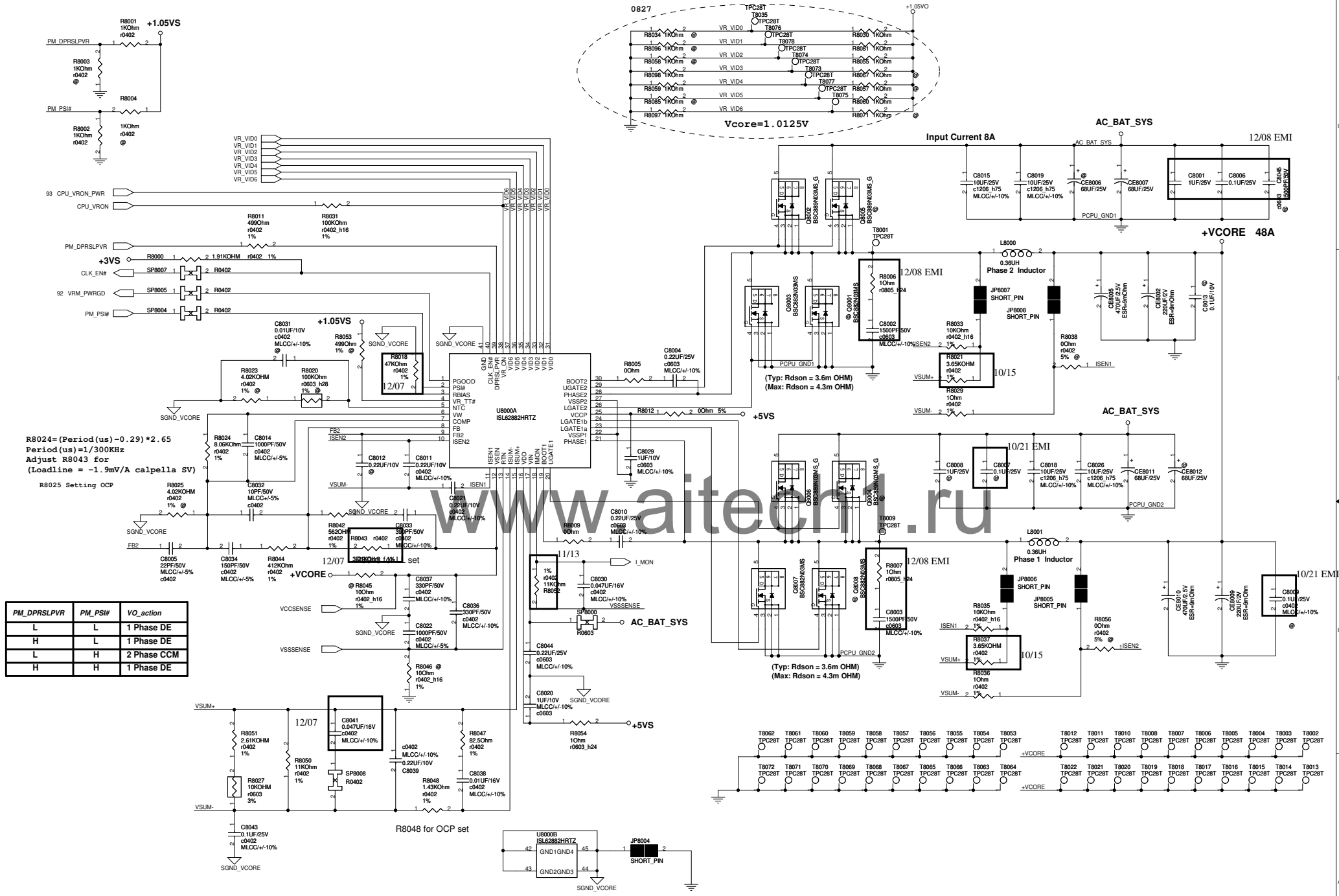
PEGATRON		Title : <Title>	
<OrgName>		Engineer: <i>Kuansheng Yang</i>	
Size	Project Name		Rev
C	H36Y_U30X10		1.0
Date: Monday, May 10, 2010		Sheet	77 of 99

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PEGATRON		Title : STRAP	
<OrgName>		Engineer: Kuansheng Yang	
Size	Project Name		Rev
C	H36Y U30X10		1.0
Date: Monday, May 10, 2010		Sheet	78 of 99

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PEGATRON		Title : <Title>	
<OrgName>		Engineer: Kuansheng Yang	
Size C	Project Name H36Y U30X10		Rev 1.0
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PM_DPRSPLVR	PM_PS#	VO_action
L	L	1 Phase DE
H	L	1 Phase DE
L	H	2 Phase CCM
H	H	1 Phase DE

$R8024 = (\text{Period}(\mu\text{s}) - 0.29) \cdot 2.65$
 $\text{Period}(\mu\text{s}) = 1/300\text{KHz}$
Adjust R8043 for
(Loadline = -1.9mV/A calpella SV)

R8025 Setting OCP

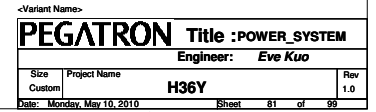
R8048 for OCP set

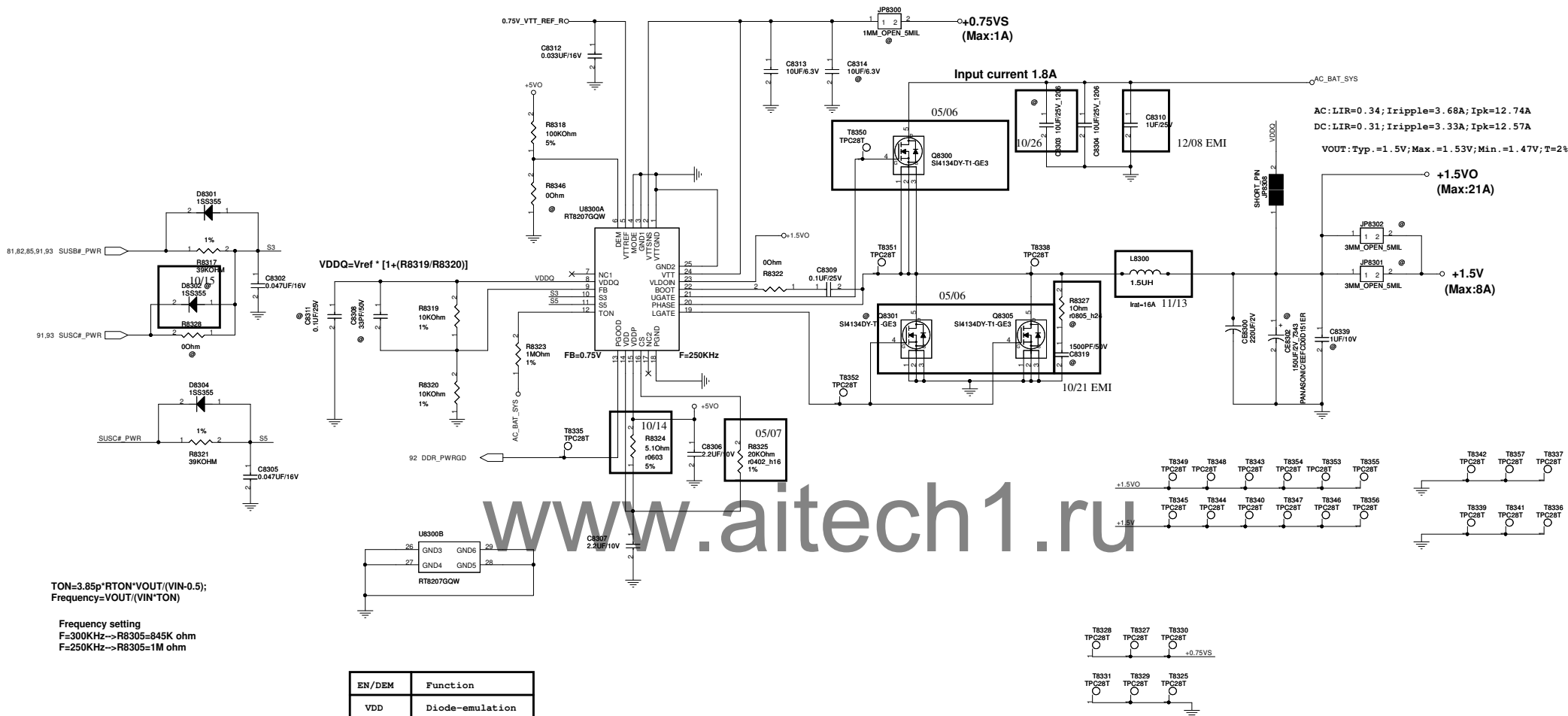
U8101B

34 GND3
35 GND4
36 GND5
37 GND6

RT8206AQW

SGND_3V_5V





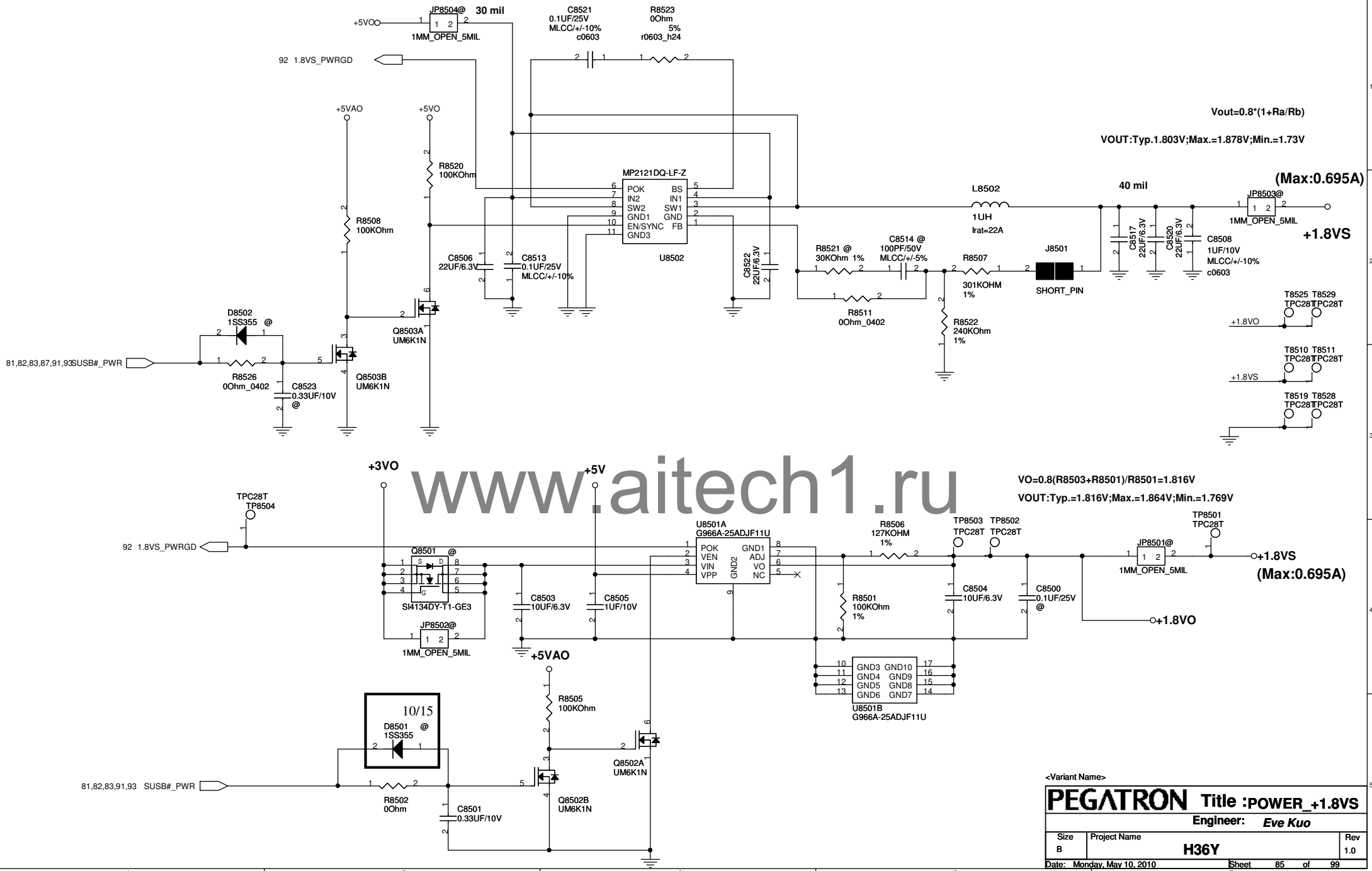
<Variant Name>

PEGATRON Title : POWER_I/O_DDR & VTT

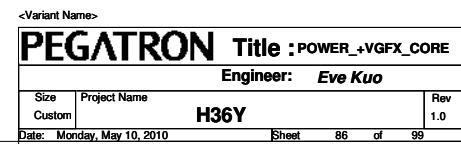
Engineer: **Eve Kuo**

Size Project Name
 Custom **H36Y** Rev 0.3
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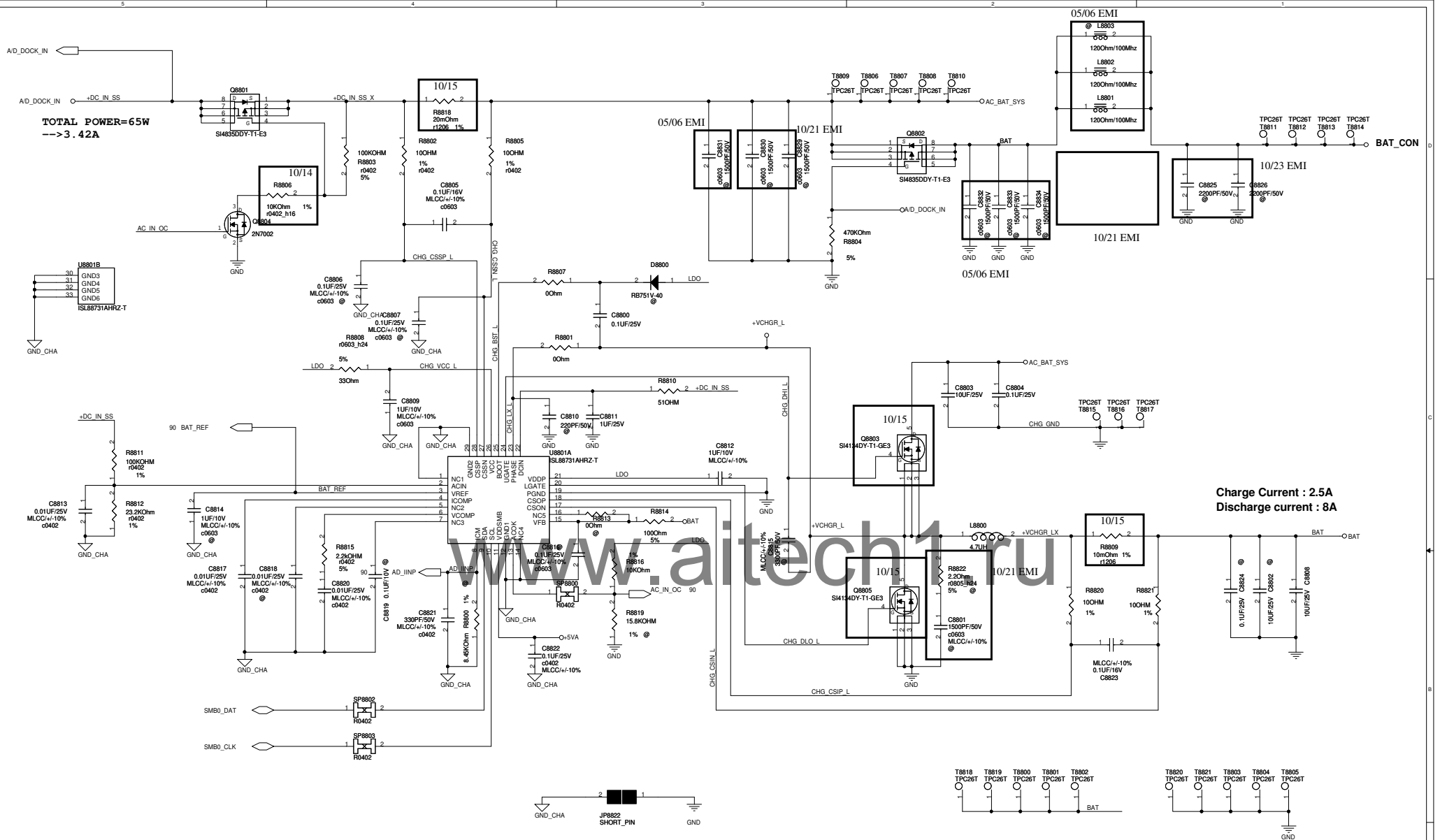


<Variant Name>			
PEGATRON Title :POWER_+1.8VS			
Engineer: Eve Kuo			
Size B	Project Name H36Y		Rev 1.0
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<Variant Name>			
PEGATRON		Title : POWER_+VGA_VCORE	
Engineer: Eve Kuo			
Size Custom	Project Name H36Y		Rev 1.0
Date: Monday, May 10, 2010		Sheet	87 of 99
1			



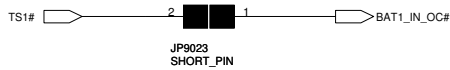
Charger IC and EC Code correlation sheet :
 Charger MAX8725 => EC CODE : 200
 Charger MAX17015 => EC CODE : 201
 Charger MB39A132 => EC CODE : 202
 Charger ISL6251 => EC CODE : 203

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<Variant Name>

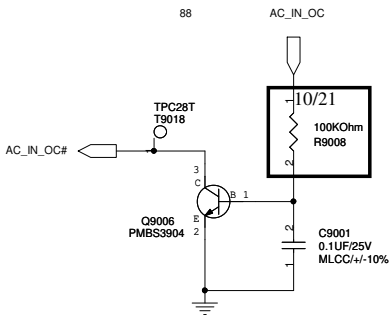
PEGATRON		Title : POWER_N/A	
Engineer: <i>Jeff_Du</i>			
Size A	Project Name N83		Rev 1.0
Date: Monday, May 10, 2010		Sheet	89 of 99

BATTERY IN DETECT



ADAPTER IN DETECT

Use MAX17015 IC function to Cost down component

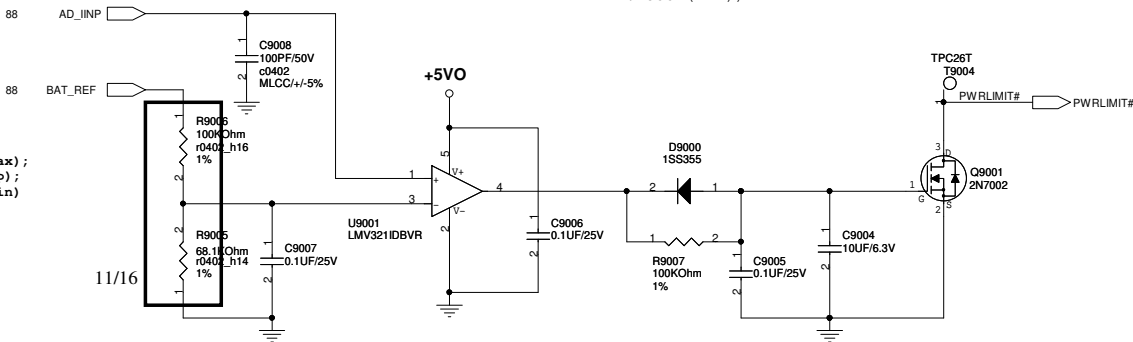


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POWER LIMIT CIRCUIT

$$\text{Pinput}=65\text{W} \rightarrow \text{Iinput}=3.25\text{A} \quad \text{R2}=20 \text{ mohm}$$
$$\text{Vicm}=20 \times \text{Iinput} \times \text{R2} \Rightarrow \text{Vicm}=1.3655\text{V}(\text{max})$$
$$1.3\text{V}(\text{typ})$$
$$1.2355\text{V}(\text{min})$$

+2.5Vref delete

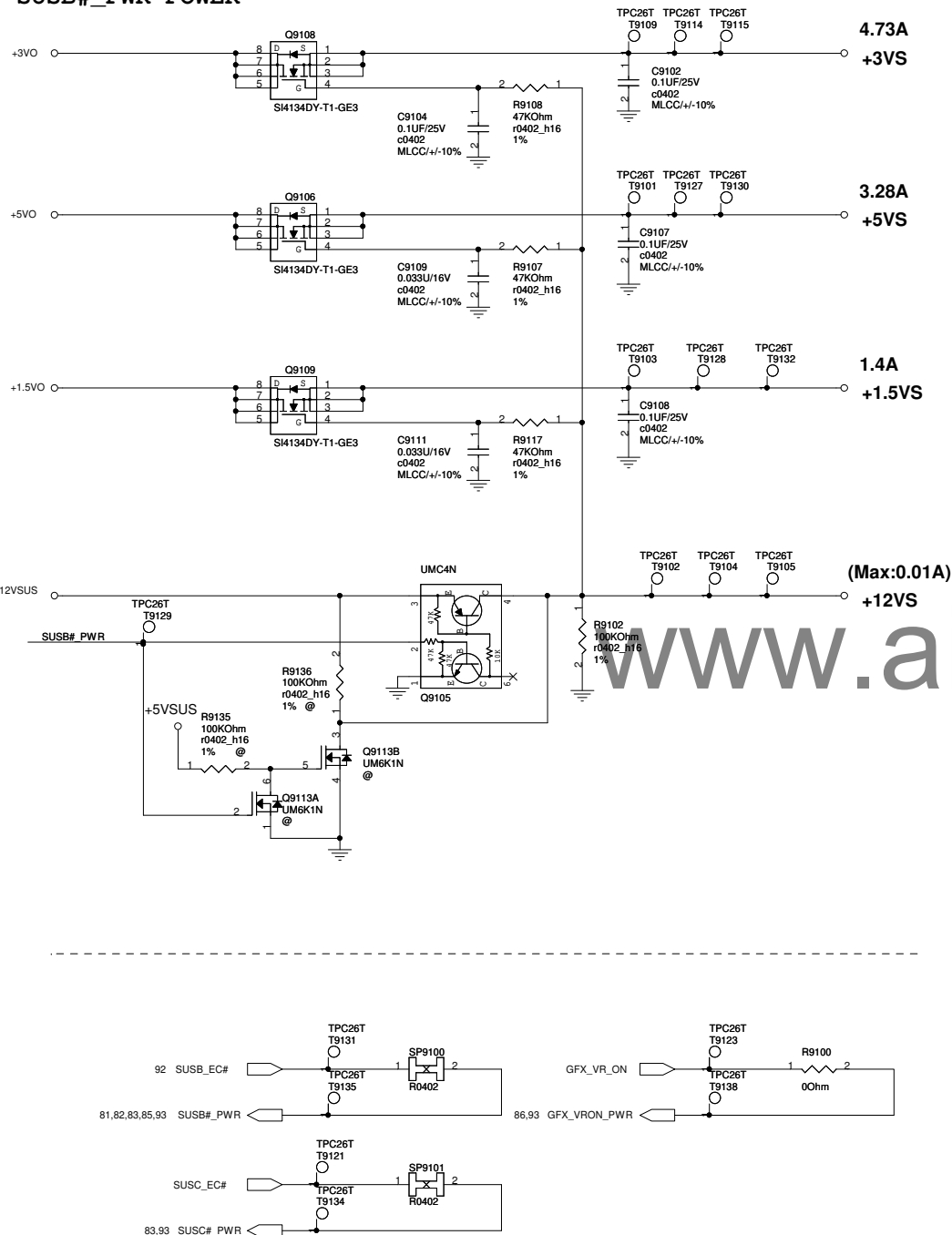
$$\text{Vref}=3.2\text{V}; \text{T}=1\%$$
$$\text{Viinp}=1.2335\text{V}(\text{Max});$$
$$1.206\text{V}(\text{Typ});$$
$$1.1793\text{V}(\text{Min})$$



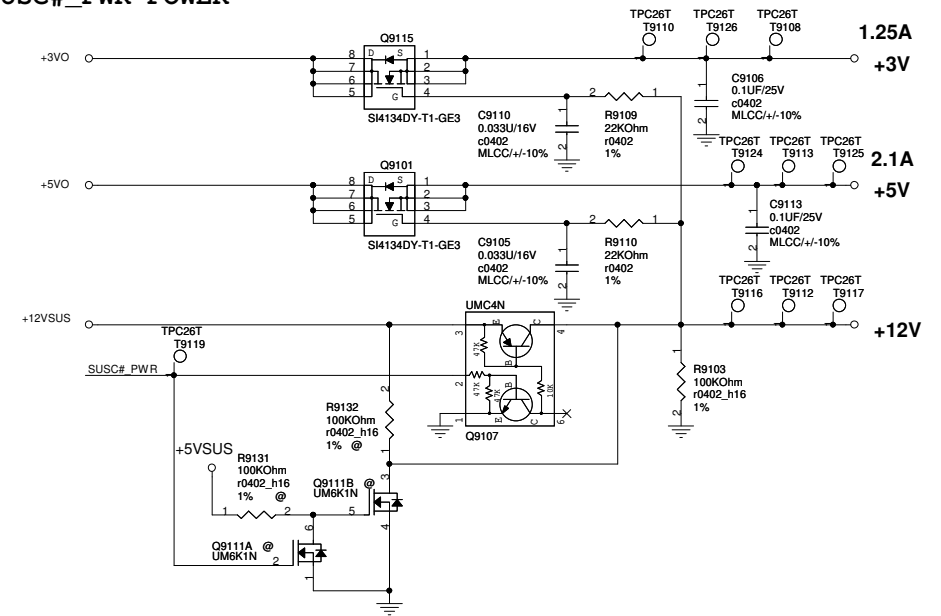
<Variant Name>

PEGATRON		Title :POWER_DETECT	
Engineer: Eve Kuo			
Size	Project Name	Rev	
Custom	H36Y	1.0	
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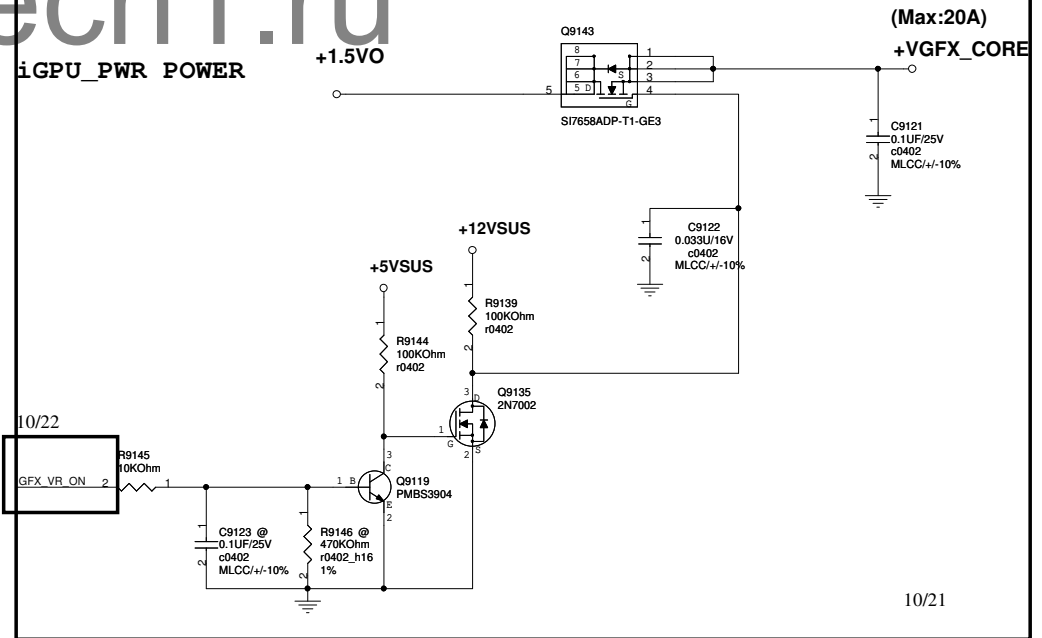
SUSB#_PWR POWER



SUSC#_PWR POWER



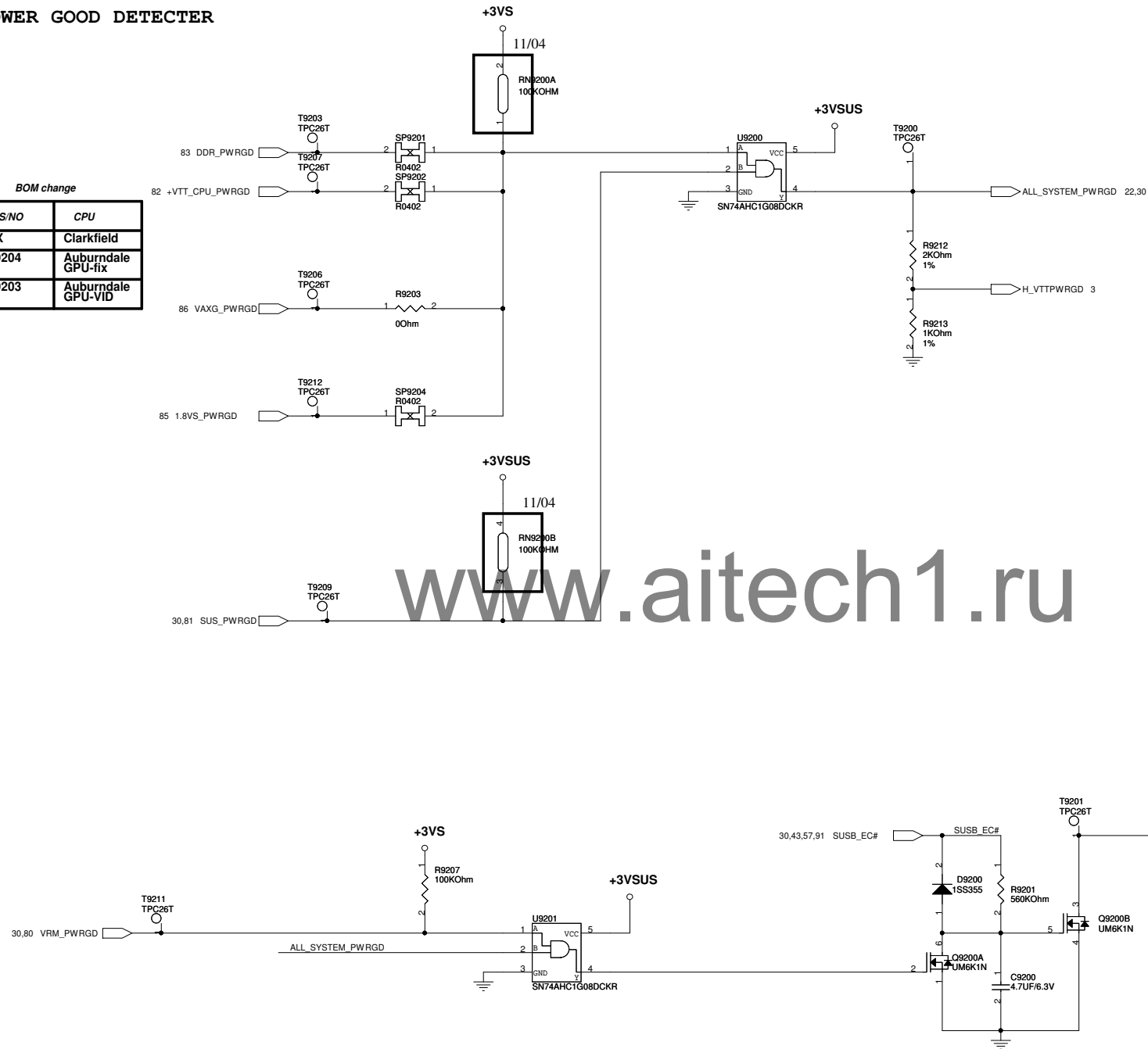
iGPU_PWR POWER



POWER GOOD DETECTER

BOM change

YES/NO	CPU
X	Clarkfield
R9204	Auburndale GPU-fix
R9203	Auburndale GPU-VID



<Variant Name>

PEGATRON Title :POWER_PROTECT
Engineer: Eve Kuo

Size	Project Name	Rev
Custom	H36Y	1.0
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AC_BAT_SYS ○ → AC_BAT_SYS 80,81,82,83,86,88
BAT ○ → BAT 88
BAT_CON ○ → BAT_CON 88

+3VA ○ → +3VA 81
+5VAO ○ → +5VAO 81,85
+5VA ○ → +5VA 81,82,88

+5VO ○ → +5VO 81,82,83,90,91
+3VO ○ → +3VO 81,85,91
+1.8VO ○ → +1.8VO 85

+1.05VO ○ → +1.05VO 80,82,86,91

+0.75VS ○ → +0.75VS 83
+1.5VO ○ → +1.5VO 83,91
+5VSUS ○ → +5VSUS 81,91
+3VSUS ○ → +3VSUS 81,92
+12VSUS ○ → +12VSUS 81,91

+5V ○ → +5V 85,91
+3V ○ → +3V 91
+12V ○ → +12V 91

+3VS ○ → +3VS 80,86,91,92
+1.5V ○ → +1.5V 83

+5VS ○ → +5VS 80,86,91
+12VS ○ → +12VS 91
+1.05VS ○ → +1.05VS 80,82

+VTT_CPU ○ → +VTT_CPU 82

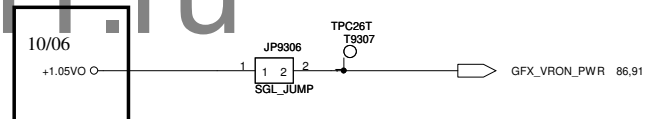
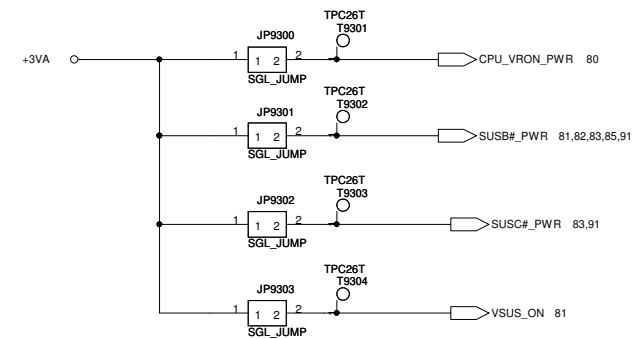
+1.5VS ○ → +1.5VS 91

+1.8VS ○ → +1.8VS 85

+VCORE ○ → +VCORE 80

+VGFX_CORE ○ → +VGFX_CORE 82,86,91

FOR POWER TEST

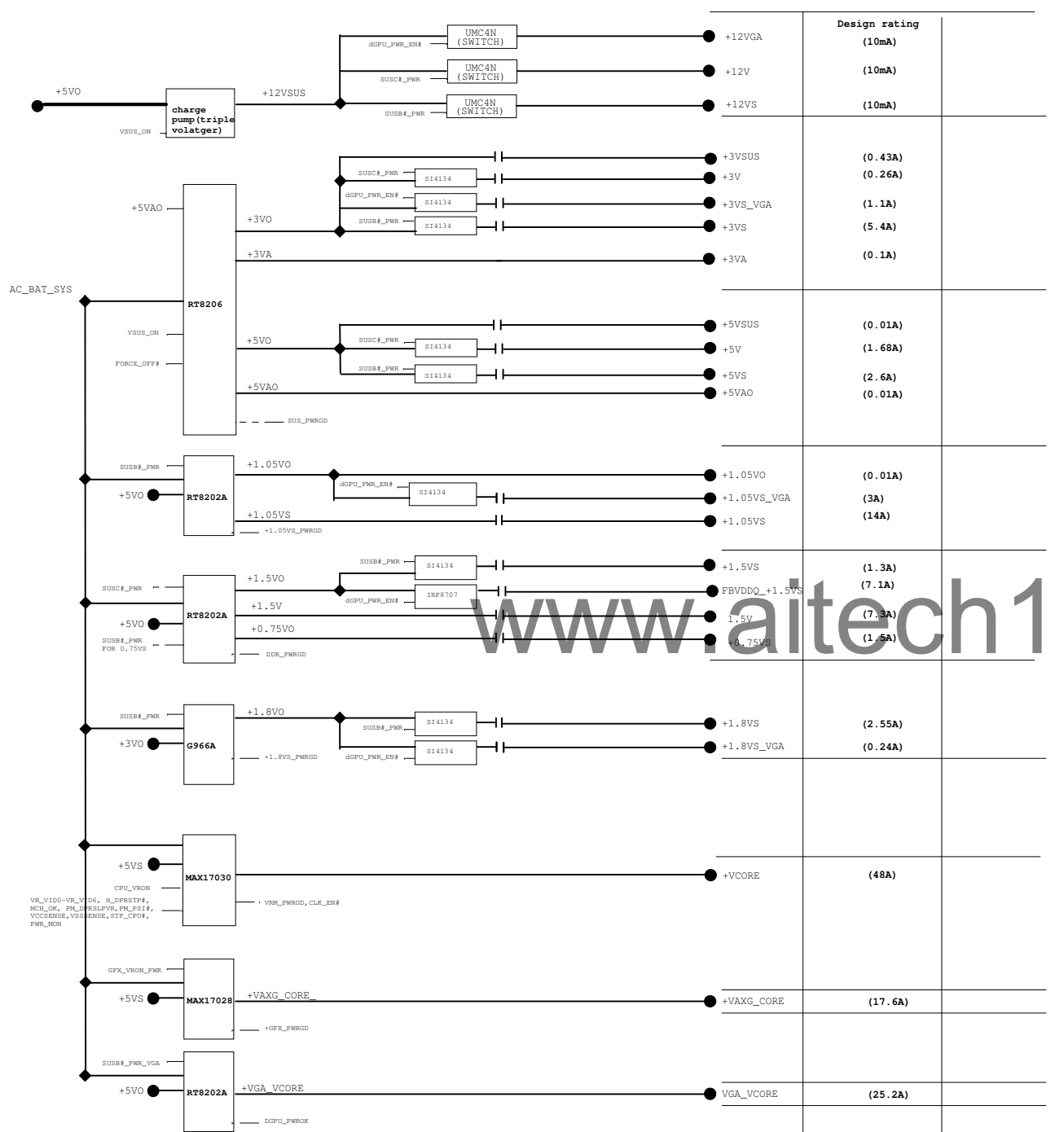


<Variant Name>

PEGATRON Title : POWER_SIGNAL
Engineer: Eve Kuo

Size	Project Name	Rev
Custom	H36Y	1.0

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modify notice

Version	Date	Description
1.0	090619	1. page88 alter solution that form MAX17015 change into ISL6251A. 2. page86 alter solution that form MAX17028 change into ISL62881.
	090622	1.Vcore form 3 Phase change into 2Phase 2.Q8100 Q8101 form SI4134DY change to SI7326 Q8102 form SI4134DY change to SI7716ADN Q8103 from SI4134DY change to SI7114ADN 3.De1 CE8104 CE8105 Q8202 Q8305 Q8602 ADD CE8712
	090623	1.De1 Q8008 Q8009 Q8203 Q8304 Q8604 ADD C8005 2.CE8103 From 150uf/4v change to 220uf/4v CE8101 From 100uf/6.3v change to 150uf/6.3v 3.Q8201 From IRF8707 change to SIR474DP Q8202 From IRF8707 change to SI7170DP L8201 From 0.56uH change 1uH CE8203 CE8204 From 470uf/2.5V change to 330uf/2.5V 4.Q8302 From IRF8707 change to SIR474DP Q8303 From IRF8707 change to SI7658ADP L8300 From 0.56uH change 1uH CE8302 CE8300 From 470uf/2.5V change to 330uf/2.5V 5.Q8603 From SI7170DP change to SI7658ADP
	090626	Modify R& C SIZE
	090629	Modify R& C SIZE UPDATE JP8801 JP8802 JP8803 JP8804 JP8805 JP8806 Part Number Change CE8005 CE8010 From NEC change to PANASONIC Modify OCP Resister R8125 R8124 R8247 R8308 R8706
	100330	Page 85 +1.8VS add co-layout PWM circuit.

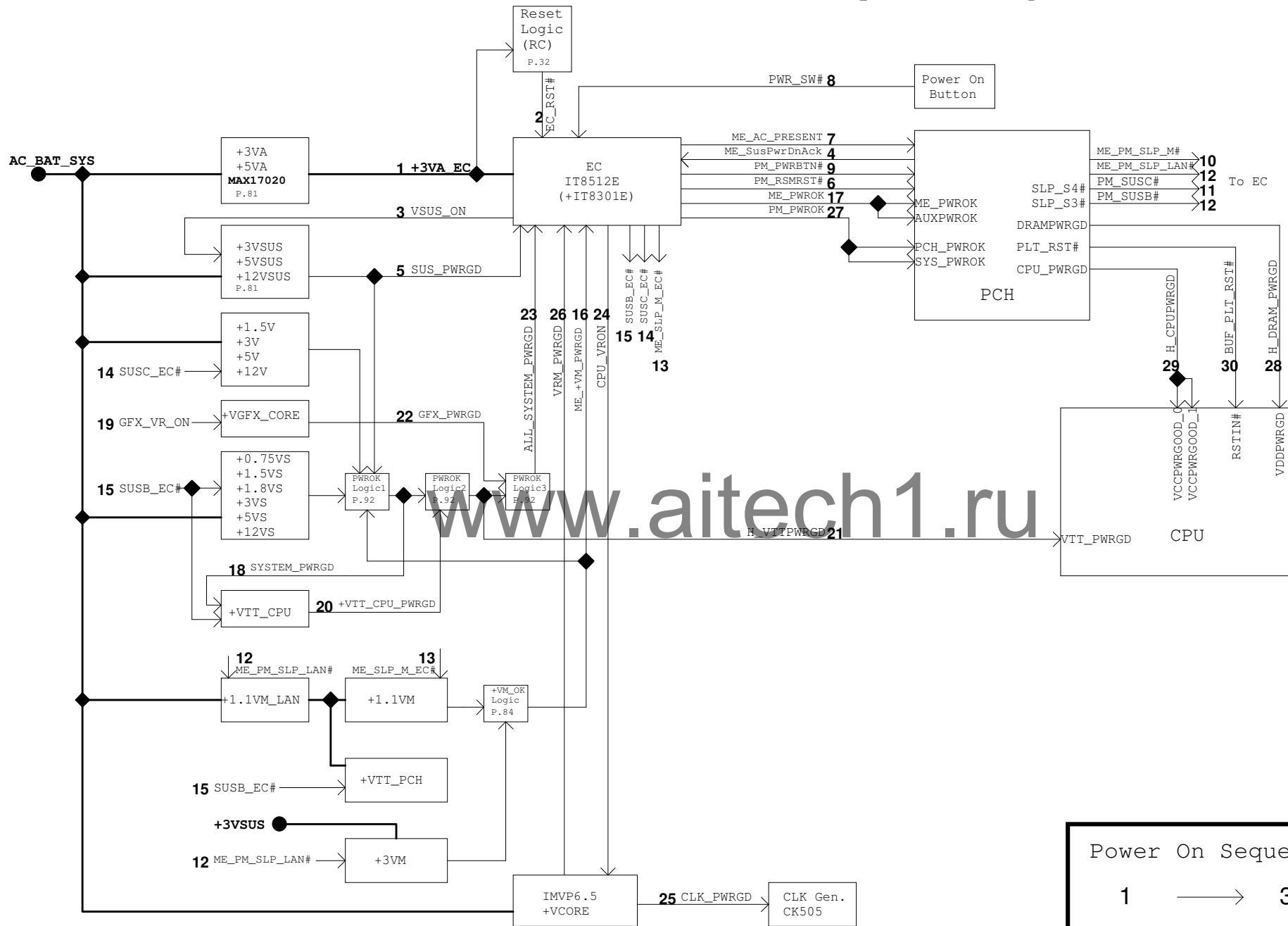
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PEGATRON		Title : <i>N/A</i>	
BG1HW1		Engineer: <i>George Chen</i>	
Size	Project Name		Rev
Custom	H26		1.0
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PEGATRON		Title : ****	
BG1HW1		Engineer: George Chen	
Size	Project Name		Rev
Custom	H26		1.0
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Power On Sequence Diagram Rev. 0.2



Power On Sequence

1 → 30

Power-On Sequence Timing Diagram Rev. 0.2



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